CHAPTER 14

SEMICONDUCTOR DEVICES AND DIGITAL CIRCUITS

14.1 ELECTRONIC DEVICES

1. *What are electronic devices ? What are their two basic types ? Give the distinguishing features of each type.*

Electronic devices. The discovery of the electron was a landmark in physics and has led to a great technological advances. The present day instant communication with the entire world is the result of the multifarious uses of these electrons.

As an electron is a light particle having a negative charge, so it can be easily manipulated with the expenditure of a small amount of energy *i.e.*, it can be made to attain high speeds and its direction can be easily changed, as desired, by means of suitable electric and magnetic fields. In fact, an electron can be made to attain speeds nearing an appreciable fraction of the speed of light in free space. This high speed makes its instant action possible.

Any *device whose action is based on the controlled flow of electrons through it is called an electronic device.* The branch of physics that deals with the study of these electronic devices is called ***electronics***. Electronic devices are the basic ***building blocks*** of all the electronic circuits.

The electronic devices are of *two* basic types :

A. Vacuum tubes. These include vacuum diodes (consisting of two electrodes – cathode and anode), triode (with three electrodes) and pentode (with 5 electrodes).

Some of the important features of vacuum tubes are as follows :

1. In vacuum tubes, electrons are obtained from a heated cathode and the flow of electrons is controlled by varying the voltage between its different electrodes.
2. A vacuum is necessary in the interelectrode region so that the electrons may not lose their energy on colliding with air molecules in their path.
3. As the electrons can flow only in one direction *i.e.*, from cathode to anode, so vacuum tubes are also known as ***vacuum valves***.
4. The vacuum tubes are bulky, consume high power and operate generally at high voltages (≈ 100 V).
5. They have limited life and low reliability.

B. Solid-state electronic devices. In 1930's, it was first realised that some solid-state semiconductors and their junctions offer the possibility of controlling the number and direction of flow of charge carriers through them. Semiconductors are the basic materials used in the present solid electronic devices like junction diode (a 2-electrode device), transistor (a 3-electrode device) and integrated circuits (ICs).

Some of the important features of the semiconductor devices are as follows :

1. In a semiconductor device, simple excitations like light, heat or small applied voltage can change the number of charge carriers.

2. The charge carriers flow in the solid itself, no vacuum has to be created for the flow of charges as required in vacuum tubes.
3. It does not require any cathode heating for the production of charge carriers. So it starts operating as soon as it is switched on.
4. Semiconductor devices are small in size, consume low power and operate at low voltages.
5. They have long life and high reliability.

For Your Knowledge

- Much before the discovery of semiconductor devices, a naturally occurring crystal *galena* (Lead sulphide : PbS) with a metal point contact attached to it was used as *detector of radiowaves*.
- The use of semiconductors to develop junction diodes and transistors has great advancement in electronics. The *miniaturisation* of various electronic gadgets became possible with the use of semiconductor devices and a continuation of this process led to the discovery of *integrated circuits*.

14.2 CLASSIFICATION OF SOLIDS ON THE BASIS OF THEIR ELECTRICAL PROPERTIES

2. *How can we classify solids on the basis of their values of electrical conductivity or resistivity ?*

Classification of solids on the basis of their electrical properties. On the basis of their relative values of electrical conductivity (σ) or resistivity ($\rho = 1/\sigma$), we can broadly classify solids into *three* categories :

A. Metals. They have very low resistivity or high conductivity.

$$\rho \approx 10^{-2} - 10^{-8}\ \Omega\text{m}$$
$$\sigma \approx 10^{2} - 10^{8}\ \text{Sm}^{-1}$$

B. Insulators. They have high resistivity or low conductivity.

$$\rho \approx 10^{8}\ \Omega\text{m}$$
$$\sigma \approx 10^{-8}\ \text{Sm}^{-1}$$

C. Semiconductors. They possess resistivity or conductivity intermediate to metals and insulators.

$$\rho \approx 10^{5} - 10^{0}\ \Omega\text{m}$$
$$\sigma \approx 10^{-5} - 10^{0}\ \text{Sm}^{-1}$$

In this chapter we are mainly concerned with semiconductors. Some of their distinguishing features are as follows :

1. Semiconductors have a much higher resistivity than metals.
2. Semiconductors have a *temperature coefficient* of resistivity (α) that is both *negative* and *high*. That is the resistivity of *semiconductors decreases* rapidly with temperature, while that of *metals increases*.
3. Semiconductors have a considerable lower number density n of charge carriers (charge carriers per unit volume) than metals.

14.3 CLASSIFICATION OF SEMICONDUCTORS

3. *How can we classify semiconductors on the basis of their chemical composition ? Give some examples of each type.*

Classification of semiconductors on the basis of their chemical composition. This scheme divides semiconductors broadly into elemental and compound semiconductors.

A. ***Elemental semiconductors*** : Si and Ge.

B. ***Compound semiconductors*** : Examples are :

(*i*) *Inorganic* : CdS, GaAs, CdSe, InP, etc.

(*ii*) *Organic polymers* : Polypyrrole, polyaniline, polythiophene, etc.

At present, both elemental and compound inorganic semiconductors are being largely used. After 1990, semiconductor devices using organic semiconductors and semiconducting polymers have been developed. This has signalled the futuristic technology of *molecular-electronics* and *polymer-electronics*.

4. *How can we classify semiconductors on the basis of the source and the nature of the charge carriers ?*

Classification of semiconductors on the basis of the source and the nature of the charge carriers. This scheme divides semiconductors into intrinsic and extrinsic semiconductors as defined below :

A. Intrinsic semiconductors. *The pure semiconductors* (impurity less than 1 part in 10^{10}) *are called intrinsic semiconductors*. The presence of the mobile charge carriers (electrons and holes) is an *intrinsic* property of the material and these charges are obtained as a result of thermal excitation. *Holes* are essentially the *electron vacancies* with an effective positive charge. In an intrinsic semiconductor, the number density of electrons (n_e) is equal to the number density of holes (n_h).

B. Extrinsic semiconductors. *The semiconductors obtained by adding or doping the pure semiconductor with small amounts of certain specific impurity atoms having valency different from that of the host atoms are called extrinsic semiconductors*. Doping drastically changes the number density of mobile electrons and holes. The electrical conductivity of such semiconductors is essentially due to the foreign atoms *i.e., extrinsic* in nature.

14.4 VALENCE BOND MODEL FOR INTRINSIC SEMICONDUCTORS

5. *On the basis of valance bond model, explain the mechanism of conduction in intrinsic semiconductors.*

Valence bond model of intrinsic semiconductors. The term intrinsic semiconductor refers to a pure semiconductor whose conductivity is due to the presence of intrinsic charge carriers (electrons and holes) and not due to any impurity or foreign atoms. Consider the crystal of semiconductor Ge or Si. Each Ge atom has four valence electrons which it shares with the four nearest neighbouring atoms to form four covalent bonds. Thus each Ge atom is tetrahedrally bonded to four neighbouring Ge atoms, as shown in Fig. 14.1. Such a crystal structure is called *diamond-like structure*. The shared pair of electrons oscillates back-and-forth between the two associated atoms. However, such a structure with all bonds intact (or no bond broken) exists at low temperature.

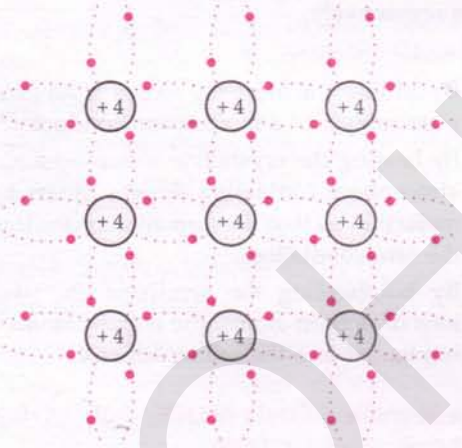


Fig. 14.1 Covalent bonding in Si or Ge. The symbol + 4 represents inner core of Ge or Si. All bonds are intact at low temperature.

As the temperature increases, the thermal energy of the valence electrons increases. As shown in Fig. 14.2, an electron may break away from the covalent bond and becomes *free* to conduct electricity. This electron leaves behind a vacancy in the covalent bond (at site 1). This vacancy of an electron with an effective *positive electronic charge is called a* ***hole***. It behaves as an *apparent free particle* with a charge $+e$. The process of setting free an electron from a covalent bond and the simultaneous creation of a hole requires a kind of *ionisation energy* E_g. The number of electrons (n_e) set free at absolute temperature T is given by

$$n_e = Ce^{-E_g/2kT}$$

where k is the Boltzmann constant. For a given E_g, clearly n_e increases as the temperature increases.

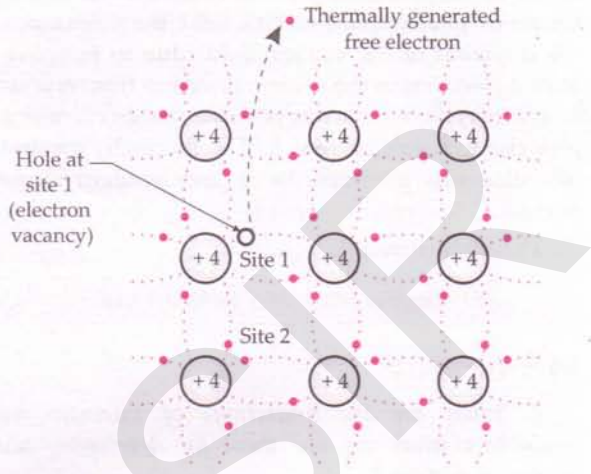


Fig. 14.2 Generation of a hole at site 1 and liberation of a free electron due to thermal energy at moderate temperature.

As each free electron creates one hole, so in an intrinsic semiconductor, the number density of free electrons (n_e) is equal to the number density of holes (n_h) and each is equal to the *intrinsic charge carrier concentration* (n_i).

$$n_e = n_h = n_i$$

6. *How do holes act as positive charge carriers ?*

Holes as positive charge carriers. Fig. 14.2 shows a hole at site 1. An electron at site 2 of the neighbouring covalent bond may jump to the site 1. After such a jump, a hole is created at site 2 and site 1 gets occupied by an electron as shown in Fig. 14.3. Apparently, the hole has moved from site 1 to site 2. Thus the motion of the hole may be regarded as the *transfer of ionisation* from one atom to another by the actual motion of the

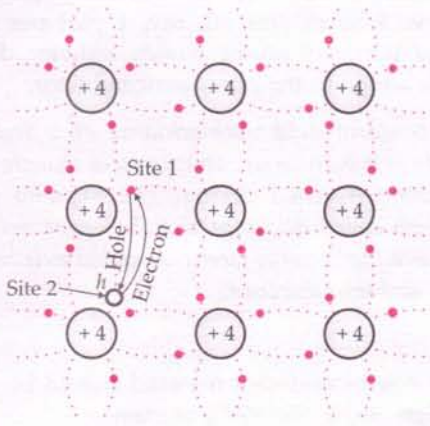


Fig. 14.3 Apparent movement of a hole in an intrinsic semiconductor.

bound electron from one covalent bond to another. Clearly, the original thermally generated free electron is not involved in this process of hole motion. Under the action of an applied electric field, the holes move in the direction of the electric field (due to jumping of bound electrons in the reverse direction from one atom to another). So they act as positive charge carriers and give rise to a hole current I_h. The thermally generated free electrons give rise to an independent electron current I_e.

The total current is

$$I = \text{Electron current} + \text{hole current} = I_e + I_h.$$

14.5 DOPING

7. *What are the limitations of intrinsic semiconductors when we use them for developing semiconductor devices ?*

Limitations of intrinsic semiconductors. When intrinsic semiconductors are used for developing semiconductor devices, they have many limitations as discussed below :

1. Intrinsic semiconductors have low intrinsic charge carrier concentration (of hole and electrons) $\approx 10^6 m^{-3}$. So they have low electrical conductivity.
2. As intrinsic charge carriers are always thermally generated, so flexibility is not available to control their number.
3. For intrinsic semiconductors, $n_e = n_h$. They cannot have predominant hole or electron conduction. This puts a limit to the usefulness of such materials.

8. *What is doping ? What are the essential requisities of doping ? Mention the various methods of doping.*

Doping. In order to increase the conductivity of pure semiconductors and to overcome their other limitations, a small amount, say, 1 part per million (ppm), of impurity atoms having valency different from 4, is added to the pure semiconductor.

The process of deliberate addition of a desirable impurity to a pure semiconductor so as to increase its conductivity is called doping. The impurity atoms added are called ***dopants*** *and the semiconductors doped with the impurity atoms are called* ***extrinsic*** *or* ***doped semiconductors***.

Essential requirements for a doping process :

1. The semiconductor material should be of very high purity, 99.9999% or more.
2. The dopant atom should neatly replace the semiconductor atom.
3. The size of the dopant atom should be almost the same as that of the semiconductor atom. For this the atoms of third and fifth group of the periodic table are most suitable.
4. The dopant atoms should not distort the crystal lattice.
5. The concentration of dopant atoms should be small, about 1 part per million.

Two types of dopants. There are two types of dopants used in doping the tetravalent Si or Ge :

(*i*) ***Pentavalent dopants.*** They have 5 valence electrons. For example, arsenic (As), antimony (Sb) and phosphorous (P).

(*ii*) ***Trivalent dopants.*** They have 3 valence electrons. For example, indium (In), boron (B) and aluminium (Al).

On doping Si or Ge with pentavalent and trivalent impurity atoms, we get two entirely different types of semiconductors, called ***n*-type** and ***p*-type** semiconductors respectively.

Methods of doping :

1. By adding the impurity atoms to an extremely pure sample of a molten semiconductor.
2. By heating the crystalline semiconductor in an atmosphere containing dopant atoms or their molecules so that the dopant atoms diffuse into the semiconductor.
3. By bombarding the semiconductor with the ions of dopant atoms, the dopant atoms can be implanted into the semiconductor.

14.6 VALENCE BOND MODEL OF EXTRINSIC SEMICONDUCTORS

9. *What are extrinsic semiconductors ? On the basis of valence bond model, explain how can a semiconductor of Ge or Si be converted into (i) n-type and (ii) p-type semiconductor ?*

Extrinsic semiconductors. *A semiconductor doped with some suitable impurity atoms so as to increase its number of charge carriers is called an extrinsic semiconductor.*

Extrinsic semiconductors are of *two* types :

1. *n*-type semiconductors.

2. *p*-type semiconductors.

1. *n*-type semiconductor. This semiconductor is obtained by doping the tetravalent semiconductor Si (or Ge) with pentavalent impurities such as As, P or Sb of group V of the periodic table. As shown in Fig. 14.4, when a pentavalent impurity atom substitutes the tetravalent Si atom, it uses four of its five valence

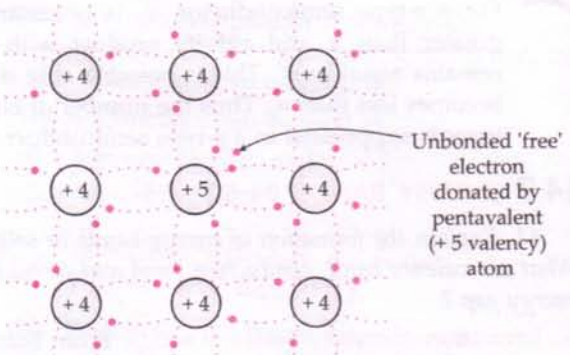


Fig. 14.4 Formation of *n*-type semiconductor by doping tetravalent Si with pentavalent impurity.

electrons in forming four covalent bonds with neighbouring Si atoms while the fifth electron is loosely bound to the impurity atom. A very small amount of ionisation energy (≈0.01 eV for Ge and 0.05 eV for Si) is required to detach this electron. At room temperature, the thermal energy is enough to set free this electron. The dopant atom gets converted into an ionised +ve core. As each pentavalent impurity atom donates one extra electron for conduction, it is called a ***donor***. These semiconductors have free electrons contributed by donors and generated by the thermal process while the holes are only due to thermal generation. Hence, the ***electrons*** are the ***majority charge carriers*** and ***holes*** are the ***minority charge carriers***. As most of the current is carried by the negatively charged electrons, so the semiconductors doped with donor type impurities are known as ***n-type semiconductors***.

For such semiconductors,

$$n_e >> n_h \quad \text{or} \quad n >> p$$

The *n*-type material can be regarded as a fixed core of one positive charge alongwith its associated electron, as shown in Fig. 14.5.

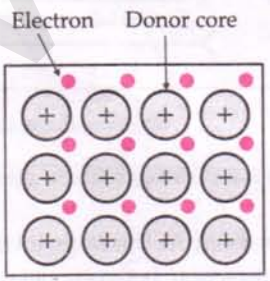


Fig. 14.5 Schematic representation of *n*-type material showing fixed cores of donors, each with one effective charge and its associated electron.

2. *p*-type semiconductor. Such a semiconductor is obtained by doping the tetravalent semiconductor Si (or Ge) with trivalent impurities such as In, B, Al or Ga. As shown in Fig. 14.6, the impurity atom uses its three valence electrons in forming covalent bonds with three neighbouring Si atoms and one covalent bond with a

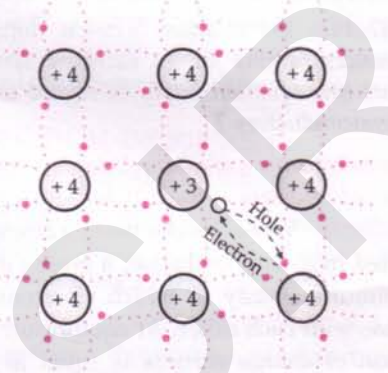


Fig. 14.6 Formation of *p*-type semiconductor by doping tetravalent Si with trivalent impurity.

neighbouring Si atom is left incomplete due to the deficiency of one electron. An electron from the neighbouring Si-Si covalent bond can slide into this vacant bond, creating a vacancy or hole in that bond. This hole is now available for conduction. The trivalent impurity atom becomes negatively charged when all its valence bonds get filled. The material can be regarded as a fixed core of one negative charge alongwith its associated hole, as shown in Fig. 14.7. The *trivalent impurity atom is called an acceptor* because it creates a hole which can accept an electron from the neighbouring bond. Obviously, there are holes created by the acceptor atoms in addition to the thermally generated holes while the free electrons are only due to thermal generation. Hence, holes are the *majority charge carriers* and *electrons* are the *minority charge carriers*. The semiconductors doped with acceptor type impurities are called ***p-type semiconductors***, because most of the

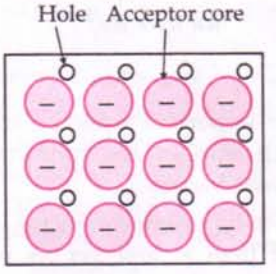


Fig. 14.7 Schematic representation of a *p*-type material showing fixed cores of acceptors, each with one effective negative charge and its associated hole.

current in these semiconductors is carried by holes which have effective positive charge. For such semiconductors,

$$n_h >> n_e \quad \text{or} \quad p >> n$$

It may be noted that doping does not disturb the overall charge neutrality of the semiconductor.

10. *Deduce the relation between different charge carrier concentrations for an extrinsic semiconductor. What does this equation imply in regard to n-type and p-type semiconductors ?*

Thermodynamic relation between the number densities of electrons and holes for an extrinsic semiconductor. When conduction electrons and holes are created in a semiconductor, a *process of destruction* occurs simultaneously in which electrons and holes recombine with each other. At equilibrium, the rate of generation of charge carriers is equal to the rate of destruction of charge carriers.

The recombination process occurs due to the collision of an electron with a hole. Larger the value of number density of electrons or holes (n_e or n_h), higher is the probability of their recombination with each other. Hence for an intrinsic semiconductor,

$$\text{Rate of recombination} \propto n_e n_h$$

or, $$\text{rate of recombination} = R n_e n_h \quad ...(1)$$

where R is a constant known as *recombination coefficient*.

For an intrinsic semiconductor, $n_e = n_h = n_i$, the intrinsic charge carrier concentration. So the equation (1) becomes

$$\text{Rate of recombination} = R n_i^2 \quad ...(2)$$

As long as the lattice structure of the semiconductor remains the same, the values of R, the rate of combination or the rate of generation (which are governed by the laws of thermodynamics) remain the same. Hence the rates of recombination given by equations (1) and (2) for extrinsic and intrinsic semiconductors must be equal. Hence

$$R n_e n_h = R n_i^2$$

or $$n_e n_h = n_i^2 \quad ...(3)$$

This is an important equation of semiconductor physics which implies the following facts of the extrinsic semiconductors :

1. For an n-type semiconductor, n_e is necessarily greater than n_i and yet its product with n_h remains equal to n_i^2. This is possible only if n_h becomes less than n_i. This implies that the number of holes gets suppressed in n-type semiconductors.
2. For a p-type semiconductor, n_h is necessarily greater than n_i and yet its product with n_e remains equal to n_i^2. This is possible only if n_e becomes less than n_i. Thus the number of electrons is suppressed in a p-type semiconductor.

14.7 ENERGY BANDS IN SOLIDS

11. *Explain the formation of energy bands in solids. What are valence band, conduction band and forbidden energy gap ?*

Formation of energy bands in solids. From Bohr's atomic model, we know that the electrons have well defined energy levels in an isolated atom. But due to interatomic interactions in a crystal, the electrons of the outer shells are forced to have energies different from those in isolated atoms. Each energy level splits into a number of energy levels forming a continuous band, called **energy band.**

An enormously large number of energy levels closely spaced in a very small energy range constitute an energy band.

Consider a small single crystal of silicon. Suppose it has N atoms. Imagine that these atoms are being brought closer from infinity so as to form a crystal of lattice spacing 'a' (2 *or* 3 Å). This is depicted in Fig. 14.8, in which the interatomic spacing is plotted along x-axis and the *energy* along y-axis.

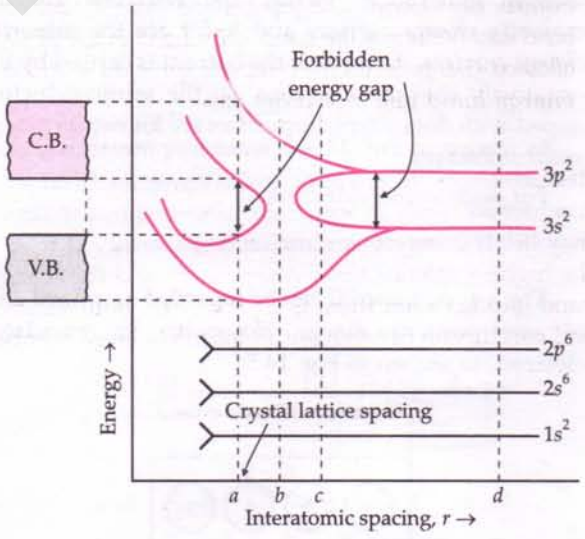


Fig. 14.8 Formation of energy bands in silicon.

1. When $r = d >> a$. At this large interatomic spacing, there is no interaction between neighbouring atoms. All the N atoms have identical energy levels. In the outer shells, N energy levels associated with 3s orbitals are completely filled with $2N$ electrons. Out of $3N$

energy levels associated with $3p$ orbitals, only N energy levels are filled with $2N$ electrons and the remaining levels are empty.

2. When $r = c >> a$ but $c < d$. As interatomic separation decreases, the valence electrons of the neighbouring atoms begin to interact. The energies of $3s$ and $3p$ levels of each atom get slightly changed (both increase and decrease). We now have N different energy levels of $3s$-type and $3N$ different levels of $3p$-type. The energy gap between $3s$ and $3p$ levels decreases. As N is very very large ($\approx 10^{23}$ atoms / cm^3), we have an enormously large number of energy levels (N of $3s$-type and $3N$ of $3p$-type) spaced in a very small energy range. *Such sets of closely spaced energy levels are called* ***energy bands.***

3. When $r = b > a$. As the separation r decreases further, the energy gap between $3s$ and $3p$ levels completely disappears and the upper and lower energy bands merge with each other. We now have a set of continuously distributed $4N$ energy levels.

4. When $r = a$. At this equilibrium separation, the band of $2N$ filled energy levels gets separated from the band of $2N$ empty energy levels by an energy gap.

The highest energy band filled with valence electrons is called ***valence band****. The lowest unfilled allowed energy band next to valence band is called* ***conduction band****. The gap between top of valence band and bottom of the conduction band in which no allowed energy levels for electrons can exist is called* ***energy band gap*** *or* ***energy gap****.*

As shown in Fig. 14.9, a solid in general, has two distinct bands of energies (called valence band and conduction band) in which the electrons in a material may lie. The lowest conduction band energy is E_c and the highest valence band energy is E_v and the energy band gap between them is $E_g = E_c - E_v$. Both valence and conduction bands have an infinitely large number of closely spaced energy levels. All energy levels in the valence band are filled while the energy levels in the conduction band may be fully empty or partially filled. According to Pauli's exclusion principle, each energy level can accommodate at the most two electrons.

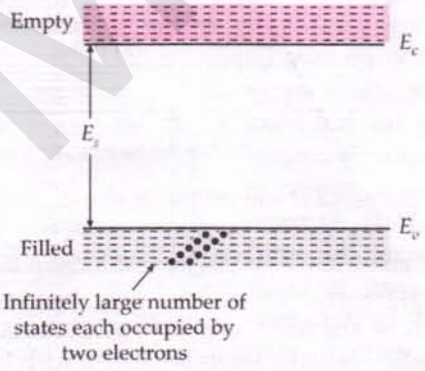


Fig. 14.9 The positions of energy bands of a solid.

14.8 DISTINCTION BETWEEN METALS, INSULATORS AND SEMICONDUCTORS ON THE BASIS OF BAND THEORY

12. *Distinguish between metals, insulators and semiconductors on the basis of band theory.*

Distinction between metals, insulators and semiconductors on the basis of band theory. Depending on the energy band gap is zero, large or small, the solids may be classified into metals, insulators and semiconductors, as explained below :

1. Metals. Here the last occupied band, called conduction band is partially filled with electrons. Two types of band structures are found in metals :

(*i*) *Either there is energy gap between the completely filled valence band and the partially filled conduction band.* As shown in Fig. 14.10[*a*(*i*)], this band structure is met in alkali metals (Li, Na, K, etc), noble metals (Cu, Ag, Au) and third group elements like Al, Ga, In and Tl.

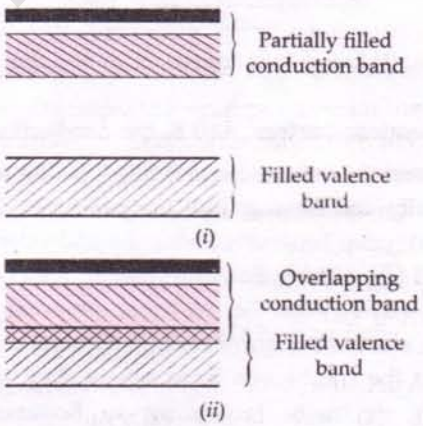


Fig. 14.10 (*a*) Energy band diagram for a metal.

(*ii*) *Or the conduction and valence bands partly overlap.* As shown in Fig. 14.10[*a*(*ii*)], this band structure is seen in metals like Be ($Z = 4 : 1s^2 2s^2$), Mg ($Z = 12 : 1s^2 2s^2 2p^6 3s^2$), Zn etc. Here the valence band is completely filled but the upper unoccupied band ($2p$ with $2s$ in Be, $3p$ with $3s$ in Mg) partly overlaps the valence band.

The highest energy level in the conduction band filled up with electrons at absolute zero is called Fermi level and the energy corresponding to the ***Fermi level*** *is called* ***Fermi Energy****.* Many electrons after gaining a slight amount

of energy from any source get excited to the empty energy levels lying immediately above the Fermi level and become free to conduct electricity. This makes available a large number of conduction electrons. So metals have low resistivity or high conductivity. Even a small electric field applied across the metal causes a current flow through it.

2. Insulators. In insulators, the valence band is completely filled while the conduction band is empty. As shown in Fig. 14.10(*b*), there is a large energy gap ($E_g > 3$ eV) between the valence and conduction bands. For example, in case of diamond, $E_g = 6$ eV. Even an electric field cannot give this much energy to an electron to make it jump from the valence band into the conduction band. Hence due to the lack of free electrons in the conduction band, the insulators are poor conductors of electricity.

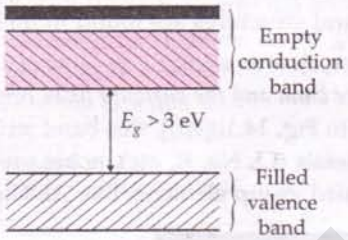


Fig. 14.10 (*b*) Energy band diagram for an insulator.

3. Semiconductors. At 0 K, the conduction band is empty and the valence band is filled. So the material is essentially insulator at low temperatures. However, the energy gap between conduction and valence bands is small ($E_g < 3$ eV). For example, $E_g = 1.17$ eV for Si and $E_g = 0.74$ eV for Ge. At room temperature, some valence electrons acquire enough thermal energy and jump to the conduction band where they are free to conduct electricity (according to Boltzmann law, number of thermally excited electrons $n \propto e^{-E_g/kT}$). Thus the semiconductor acquires a small conductivity at room temperature. The resistance of a semiconductor would not be as high as that of insulator.

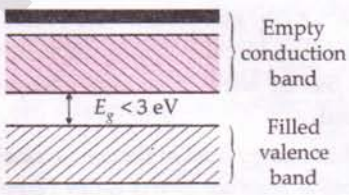


Fig. 14.10 (*c*) Energy band diagram for a semiconductor.

14.9 ENERGY BANDS OF INTRINSIC AND EXTRINSIC SEMICONDUCTORS

13. *Sketch and explain the energy band diagrams of intrinsic and extrinsic semiconductors.*

Energy band diagram of intrinsic semiconductors. At $T = 0$ K, the valence band of a semiconductor is completely filled with electrons while the conduction band is empty, as shown in Fig. 14.11[a(*i*)]. Hence an intrinsic semiconductor behaves like an insulator at $T = 0$ K. At higher temperatures ($T > 0$ K), some electrons of the valence band gain sufficient thermal

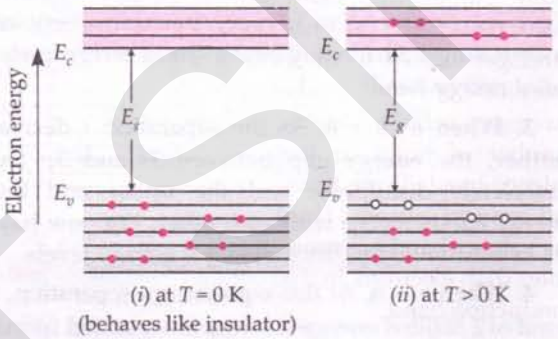


Fig. 14.11 (*a*) Energy band diagrams of intrinsic semiconductor

energy and jump to the conduction band, creating an equal number of holes in the valence band. These thermally excited electrons occupy the lowest possible energy levels in the conduction band. Therefore, the energy band diagram of an intrinsic semiconductor at $T > 0$ K is of the type shown in Fig. 14.11[*a*(*ii*)]. Clearly, the number of electrons in conduction band is equal to the number of holes in valence band.

Energy band diagram of *n*-type semiconductor. In *n*-type semiconductors, the extra (fifth) electron is very weakly attracted by the donor impurity. A very small energy (≈ 0.01 eV) is required to free this electron from the donor impurity. When freed, this electron will occupy the lowest possible energy level in the conduction band *i.e.*, the energy of the donor electron is slightly less than E_c. Thus *the donor energy level E_D lies just below the bottom of the conduction band* as shown in Fig. 14.11(*b*). At room temperature this small energy gap is easily covered by the thermally excited electrons. The conduction band has more

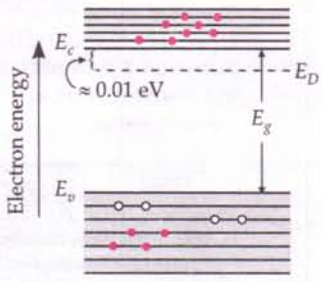


Fig. 14.11 (*b*) Energy band diagram of *n*-type semiconductor at $T > 0$ K

electrons (than holes in valence band) as they have been contributed both by thermal excitation and donor impurities.

Energy band diagram of *p*-type semiconductors. In *p*-type semiconductors, each acceptor impurity creates a hole which can be easily filled by an electron of Si-Si covalent bond *i.e.*, a very small energy ($\approx 0.01 - 0.05$ eV) is required by an electron of the valence band to move into this hole. Hence the acceptor energy level E_A lies slightly above the top of the valence band, as shown in Fig. 14.11(*c*). At room temperature, many electrons of the valence band get excited to these acceptor energy levels, leaving behind equal number of holes in the valence band. These holes can conduct current. Thus the valence band has more holes than electrons in the conduction band.

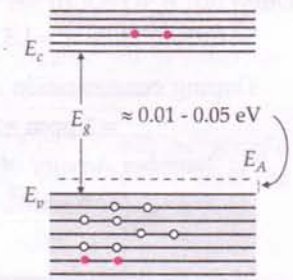


Fig. 14.11 (*c*) Energy band diagram of *p*-type semiconductor at $T > 0$ K.

14.10 DIFFERENCE BETWEEN INTRINSIC AND EXTRINSIC SEMICONDUCTORS

14. *Distinguish between intrinsic and extrinsic semiconductors.*

Intrinsic Semiconductors	Extrinsic Semiconductors
1. These are pure semiconducting tetravalent crystals.	These are semi-conducting tetravalent crystals doped with impurity atoms of group III or V.
2. Their electrical conductivity is low.	Their electrical conductivity is high.
3. There is no permitted energy state between valence and conduction bands.	There is permitted energy state of the impurity atom between valence and conduction bands.
4. The number of free electrons in the conduction band is equal to the number of holes in valence band.	The electrons are majority charge carriers in *n*-type semiconductors while holes are majority charge carries in *p*-type semiconductors.
5. Their electrical conductivity depends on temperature.	Their electrical conductivity depends on temperature as well as on dopant concentration.

14.11 DIFFERENCE BETWEEN *n*-TYPE AND *p*-TYPE SEMICONDUCTORS

15. *Distinguish between n-type and p-type semiconductors.*

n-type semiconductors	*p*-type semiconductors
1. These are extrinsic semiconductors obtained by doping impurity atoms of group V to Ge or Si crystal.	These are extrinsic semiconductors obtained by doping impurity atoms of group III to Ge or Si crystal.
2. The impurity atoms added provide free electrons and are called donors.	The impurity atoms added create vacancies of electrons (or holes) and are called acceptors
3. The donor impurity level lies just below the conduction band.	The acceptor impurity level lies just above the valence band.
4. The electrons are majority charge carriers while holes are minority charge carriers.	The holes are majority charge carriers while electrons are minority charge carriers.
5. The free electron density is much greater than hole density, *i.e.*, $n_e >> n_h$.	The hole density is much greater than free electron density, *i.e.*, $n_h >> n_e$.

14.12 HOLES

16. *What are holes ? Give their important characteristics.*

Holes. *The vacancy or absence of an electron in the bond of a covalently bonded crystal is called a hole.* In terms of band theory, whenever an electron is removed from the completely filled valence band of a semiconductor, a vacancy is left behind in the valence band. This vacancy serves as a positive charge carrier and is called a hole.

A hole is not a physical entity. A hole is a convenient way of describing charge motion, though the motion can be described entirely in terms of electrons.

Characteristics of holes :

1. A hole is just a vacancy created by the removal of an electron from a covalent bond of semiconductor.
2. It has the same mass as the (removed) electron.
3. It is associated with a positive charge of magnitude *e*.
4. The energy of a hole is higher, the farther below it is from the top of the valence band. For explanation, see short answer conceptual problem 9 on page 14.71.

Examples based on
Intrinsic and Extrinsic Semiconductors

Formulae Used

1. In an intrinsic semiconductor, $n_e = n_h = n_i$.
2. At equilibrium in any semiconductor, $n_e n_h = n_i^2$.
3. In an n-type semiconductor, $N_D \simeq n_e >> n_h$.
4. In a p-type semiconductor, $N_A \simeq n_h >> n_e$.
5. Minimum energy required to create a hole-electron pair,

$$E_g = h\nu_{min} = \frac{hc}{\lambda_{max}}$$

Units Used

Number densities n_e, n_h and n_i are in m^{-3}.

Example 1. *In a pure semiconductor, the number of conduction electrons is 6×10^{18} per cubic metre. How many holes are there in a sample of size 1 cm × 1 cm × 1 mm ?*

Solution. Here $n_e = 6 \times 10^{18} m^{-3}$

Volume of the sample

$= 1\text{ cm} \times 1\text{ cm} \times 1\text{ mm} = 10^{-7} m^3$

Number of holes in the sample

= Number of electrons in the sample

$= n_e \times V = 6 \times 10^{18} \times 10^{-7} = \mathbf{6 \times 10^{11}}$.

Example 2. *Find the maximum wavelength of electromagnetic radiation which can create a hole-electron pair in germanium. The band gap in germanium is 0.65 eV.*

Solution. Here $E_g = 0.65\text{ eV} = 0.65 \times 1.6 \times 10^{-19}$ J

This is the minimum energy required to push an electron from valence to conduction band or to create a hole-electron pair. Hence required maximum wavelength λ_{max} is given by

$$E_g = \frac{hc}{\lambda_{max}}$$

or $$\lambda_{max} = \frac{hc}{E_g}$$

$$= \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{0.65 \times 1.6 \times 10^{-19}}$$

$$= \mathbf{1.9 \times 10^{-6}\ m}.$$

Example 3. *A p-type semiconductor has acceptor levels 57 meV above the valence band. Find the maximum wavelength of light that can create a hole.*

Solution. To create a hole, an electron of valence band has to be excited into one of the acceptor levels which are 57 meV above the valence band. Hence a minimum of 57 meV energy is needed to create a hole.

As $$E_{min} = \frac{hc}{\lambda_{max}}$$

$$\therefore \quad \lambda_{max} = \frac{hc}{E_{min}} = \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{57 \times 1.6 \times 10^{-22}}$$

$$= \mathbf{2.17 \times 10^{-5}\ m}.$$

Example 4. *Suppose a pure Si crystal has 5×10^{28} atoms m^{-3}. It is doped by 1 ppm concentration of pentavalent As. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16} m^{-3}$.* [NCERT ; CBSE D 07C]

Solution. Here $n_i = 1.5 \times 10^{16} m^{-3}$

Doping concentration of pentavalent As atoms

= 1 ppm = 1 part per million

$\therefore$ Number density of pentavalent As atoms,

$$N_D = \frac{5 \times 10^{28}}{10^6} = 5 \times 10^{22}\text{ atom m}^{-3}$$

Now, the thermally generated electrons ($n_i \propto 10^{16} m^{-3}$) are negligibly small as compared to those produced by doping, so

$$n_e \simeq N_D = \mathbf{5 \times 10^{22}\ m^{-3}}$$

Also, $$n_e n_h = n_i^2$$

$$\therefore \quad n_h = \frac{n_i^2}{n_e} = \frac{1.5 \times 10^{16} \times 1.5 \times 10^{16}}{5 \times 10^{22}}$$

$$= \mathbf{4.5 \times 10^9\ m^{-3}}.$$

Example 5. *A semiconductor has equal electron and hole concentration of $6 \times 10^8 m^{-3}$. On doping with certain impurity, electron concentration increases to $9 \times 10^{12} m^{-3}$. (i) Identify the new semiconductor obtained after doping. (ii) Calculate the new hole concentration. (iii) How does the energy gap vary with doping ?* [CBSE D 05]

Solution. (*i*) As the electron concentration increases after doping, so the new semiconductor obtained is of n-type.

(*ii*) As $n_e\ n_h = n_i^2$

$$\therefore \quad n_h = \frac{n_i^2}{n_e} = \frac{(6 \times 10^8)^2}{9 \times 10^{12}} = \mathbf{4 \times 10^4\ m^{-3}}.$$

(*iii*) The energy gap decreases with doping.

Example 6. *A semiconductor has equal electron and hole concentration of $2 \times 10^8 m^{-3}$. On doping with a certain impurity, the hole concentration increases to $4 \times 10^{10} m^{-3}$. (i) What type of semiconductor is obtained on doping ? (ii) Calculate the new electron concentration of the semiconductor. (iii) How does the energy gap vary with doping ?* [CBSE D 01]

Solution. (*i*) As the hole concentration increases, the p-type semi-conductor is obtained after doping.

(*ii*) As $n_e\, n_h = n_i^2$

$$\therefore \quad n_e = \frac{n_i^2}{n_h} = \frac{(2\times10^8)^2}{4\times10^{10}} = \mathbf{10^6\ m^{-3}}.$$

(*iii*) Energy gap decreases with doping.

Problems for Practice

1. If the energy of a photon of sodium light (λ = 589 nm) equals the band gap of a semiconductor, calculate the minimum energy required to create hole-electron pair. (Ans. 2.1 eV)
2. A doped semiconductor has impurity levels 30 meV below the conduction band. Is the material *n*-type or *p*-type ? Find the maximum wavelength of light so that an electron of impurity level is just able to jump into conduction band. (Ans. 4.125×10^{-5} m)
3. The band gap of an alloy semiconductor gallium arsenide phosphide is 1.98 eV. Calculate the wavelength of radiation that is emitted when electrons and holes in this material combine directly. What is the colour of the emitted radiation ? Take $h = 6.6\times10^{-34}$ Js. (Ans. 6250 Å, red)
4. Pure silicon at 300 K has equal electron and hole concentrations of 1.5×10^{16} / m^3. Doping by indium increases the hole concentration to 4.5×10^{22} / m^3. Calculate the new electron concentration in the doped silicon. **[IPUEE 08 ; VMMC 13]**
(Ans. 5×10^9 m^{-3})

HINTS

1. $$E = E_g = \frac{hc}{\lambda} = \frac{6.6\times10^{-34}\times3\times10^8}{589\times10^{-9}}\ \text{J}$$
$$= \frac{6.6\times3\times10^{-17}}{589\times1.6\times10^{-19}}\ \text{eV} = \mathbf{2.1\ eV.}$$

2. Excitation of electrons from the impurity level to the conduction band increases electron density in the conduction band. As electrons are the majority charge carriers, so the material is *n*-type.
$$\lambda_{max} = \frac{hc}{E}$$
$$= \frac{6.6\times10^{-34}\times3\times10^8}{30\times1.6\times10^{-22}}$$
$$= \mathbf{4.125\times10^{-5}\ m.}$$

3. Use the relation, $\lambda = \dfrac{hc}{E_g}$

4. $n_i = 1.5\times10^{16}\,\text{m}^{-3}$, $n_h = 4.5\times10^{22}\,\text{m}^{-3}$
$$n_e = \frac{n_i^2}{n_h} = \frac{(1.5\times10^{16})^2}{4.5\times10^{22}} = \mathbf{5\times10^9\ m^{-3}}.$$

14.13 MOBILITY OF A CHARGE CARRIER

17. *Define electrical mobility of a charge carrier. Why is the mobility of an electron in the conduction band of a semiconductor is more than the mobility of a hole (or electron) in the valence band ?*

Electrical mobility. *The drift velocity acquired by a charge carrier in a unit electric field is called its electrical mobility and is denoted by* μ. In a semiconductor,

Drift velocity of a charge carrier $\propto$ Applied electric field

or $v \propto E$ or $v = \mu E$ $\therefore$ $\mu = \dfrac{v}{E}$

Hence, the electrical mobility μ *is the drift velocity per unit electric field.*

The mobility of an electron in the conduction band of a semiconductor is greater than the mobility of a hole in the valence band. The electrons in the conduction band are almost free. They get easily accelerated by an electric field. But the electrons in the valence band are bound between the atoms of a semiconductor. They are less accelerated by an electric field and so acquire drift velocity smaller than that of electrons in the conduction band. The mobility of electrons in the valence band is less than the mobility of electrons in the conduction band. As the motion of an electron in the valence band is equivalent to the motion of a hole in the opposite direction, hence the mobility of hole in the valence band is smaller than the mobility of an electron in conduction band.

14.14 ELECTRICAL CONDUCTIVITY OF A SEMICONDUCTOR

18. *Using the concept of electron and hole current, derive expression for the conductivity of a semiconductor.*

Electrical conductivity of a semiconductor. Consider a block of semiconductor of length *l*, area of cross- section *A*, and having free electron density n_e

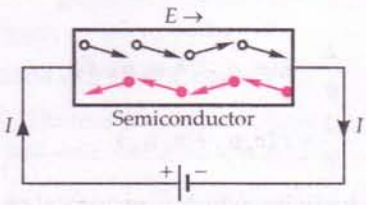


Fig. 14.12 Drifting of electrons and holes in a semiconductor on application of voltage *V*.

and hole density n_h. Suppose a potential difference *V* is applied across its ends. The electric field set up inside it will be

$$E = \frac{V}{l} \qquad ...(1)$$

Electrons begin to drift with velocity v_e in the opposite direction of E while the holes drift in the direction of E with velocity v_h, as shown in Fig. 14.12.

$\therefore$ Total current = Electron current + Hole current

or $$I = I_e + I_h \quad ...(2)$$

As electrons in the conduction band and holes in the valence band move randomly like free electrons in metals, therefore we can write

$$I_e = e\, n_e\, A\, v_e \text{ and } I_h = e\, n_h\, A\, v_h$$

$$\therefore \quad I = e\, n_e\, A\, v_e + e\, n_h\, A\, v_h$$

$$= e\, A(n_e\, v_e + n_h\, v_h) \quad ...(3)$$

If R is the resistance of the semiconductor block and ρ its resistivity, then

$$R = \rho \frac{l}{A} \quad ...(4)$$

If the applied electric field E is low, the semiconductors obey Ohm's law so that

$$I = \frac{V}{R} = \frac{El}{\rho l / A} \quad \text{[By using (1) and (4)]}$$

or $$I = \frac{EA}{\rho} \quad ...(5)$$

From equations (3) and (5), we get

$$I = \frac{EA}{\rho} = e\, A\,(n_e v_e + n_h v_h) \quad ...(6)$$

or $$\frac{E}{\rho} = e\,(n_e v_e + n_h v_h)$$

As mobility μ is defined as drift velocity per unit electric field, therefore

Electron mobility,

$$\mu_e = \frac{v_e}{E} \quad \text{or} \quad v_e = \mu_e E$$

Hole mobility,

$$\mu_h = \frac{v_h}{E} \quad \text{or} \quad v_h = \mu_h E$$

Hence

$$\frac{E}{\rho} = e\,(n_e \mu_e E + n_h \mu_h E)$$

or $$\frac{1}{\rho} = e\,(n_e \mu_e + n_h \mu_h)$$

The conductivity, which is reciprocal of resistivity, is given by

$$\sigma = \frac{1}{\rho} = e\,(n_e \mu_e + n_h \mu_h) \quad ...(7)$$

Also, the resistivity of the semiconductor is given by

$$\rho = \frac{1}{e\,(n_e \mu_e + n_h \mu_h)}. \quad ...(8)$$

14.15 EFFECT OF TEMPERATURE ON THE CONDUCTIVITY OF SEMICONDUCTORS

19. *Explain the variation of conductivity of a semiconductor with temperature.*

Variation of conductivity of a semiconductor with temperature. The conductivity of a semiconductor is given by

$$\sigma = e\,(n_e\, \mu_e + n_h\, \mu_h)$$

As the temperature increases, the mobilities μ_e and μ_h of electrons and holes decrease due to the increase in their collision frequency. But due to the small energy gap of semiconductors, more and more electrons [$n \propto e^{-E_g/kT}$] from the valence band cross over to the conduction band. The increase in carrier concentrations, n_e and n_h is so large that the decrease in the values of μ_e and μ_h has no influence. The overall effect is that the conductivity increases or the resistivity decreases with the increase of temperature.

14.16 PHOTOCONDUCTIVITY

20. *What is photoconductivity ?*

Photoconductivity. If an intrinsic semiconductor is exposed to light radiations of energy $h\nu$ greater than the band gap E_g, the electrons from the valence band jump to the conduction band. More electron-hole pairs are created. The number of electrons and hole increases. This increases the conductivity of the semiconductor. *The increase in the conductivity of a semiconductor as a result of incident photons of suitable energy is called photoconductivity.*

Semiconductors having large photoconductivity are used as *light dependent resistors* (LDR) in automatic light control circuits.

Examples Based on
Conductivity of Semiconductors

Formulae Used

1. Mobility of a charge carrier, $\mu = \frac{v}{E}$.
2. Electric current, $I = eA\,(n_e v_e + n_h v_h)$.
3. Electrical conductivity, $\sigma = \frac{1}{\rho} = e\,(n_e \mu_e + n_h \mu_h)$.
4. Variation of conductivity with temperature,
$$\sigma = \sigma_0 \exp\left(-\frac{E_g}{2k_B T}\right).$$

Units Used

Current I is in ampere, area A in m^2, conductivity σ in Sm^{-1}, resistivity ρ in Ωm, mobility μ in $m^2\, V^{-1} s^{-1}$.

Example 7. *A semiconductor is known to have an electron concentration of 8×10^{13} per cm^3 and a hole concentration of 5×10^{12} per cm^3. (a) Is the semiconductor n-type or p-type ? (b) What is the resistivity of the sample if the electron mobility is 23,000 cm^2 / Vs and hole mobility is 100 cm^2 / Vs ?*

Solution. Here $n_e = 8 \times 10^{13} \text{cm}^{-3}$, $n_h = 5 \times 10^{12}\ \text{cm}^{-3}$, $\mu_e = 23{,}000\ \text{cm}^2\ \text{V}^{-1}\text{s}^{-1}$, $\mu_h = 100\ \text{cm}^2\ \text{V}^{-1}\text{s}^{-1}$

(*a*) As $n_e > n_h$, the semiconductor must be ***n*-type**.

(*b*) Resistivity,

$$\rho = \frac{1}{e(n_e \mu_e + n_h \mu_h)}$$

$$= \frac{1}{1.6 \times 10^{-19}(8 \times 10^{13} \times 23 \times 10^3 + 5 \times 10^{12} \times 10^2)} \Omega\text{cm}$$

$$= \frac{1}{1.6 \times 10^{-19}(184 \times 10^{16} + 5 \times 10^{14})} \Omega\ \text{cm}$$

$$= \frac{1}{1.6 \times 10^{-5} \times 18405} \Omega\ \text{cm} = \mathbf{3.395\ \Omega\ cm}.$$

Example 8. *Determine the number density of donor atoms which have to be added to an intrinsic germanium semiconductor to produce an n-type semiconductor of conductivity $5\,\Omega^{-1}\ cm^{-1}$, given that the mobility of electron in n-type Ge is 3900 cm^2 / Vs. Neglect the contribution of holes to conductivity.*

Solution. Here $\sigma = 5\,\Omega^{-1}\text{cm}^{-1}$,

$$\mu_e = 3900\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}, \quad n_e = ?$$

If we neglect the contribution of holes to conductivity, then

$$\sigma = \frac{1}{\rho} = e n_e \mu_e$$

$\therefore$ Electron density,

$$n_e = \frac{\sigma}{e\mu_e} = \frac{5}{1.6 \times 10^{-19} \times 3900}\ \text{cm}^{-3}$$

$$= \mathbf{8.01 \times 10^{15}\ cm^{-3}}.$$

Example 9. *A battery of emf 2 V is connected across a block of length 0.1 m and area of cross-section $1 \times 10^{-4}\ m^2$. If the block is of intrinsic silicon at 300 K, find the electron and hole currents. What will be the magnitude of the total current ? What will be the magnitude of the total current if germanium is used instead of silicon ?*

Given that for Si at 300 K : $\mu_e = 0.135\ m^2V^{-1}s^{-1}$, $\mu_h = 0.048\ m^2V^{-1}s^{-1}$ *and intrinsic carrier concentration* $n_i = 1.5 \times 10^{16} m^{-3}$.

For Ge at 300 K : $\mu_e = 0.39\ m^2V^{-1}s^{-1}$, $\mu_h = 0.19\ m^2V^{-1}s^{-1}$ *and* $n_i = 2.4 \times 10^{19} m^{-3}$.

Solution. Here $A = 10^{-4}\ \text{m}^2$, $l = 0.1\ \text{m}$, $V = 2\ \text{V}$

Electric field set up in the block is

$$E = \frac{V}{l} = \frac{2\ \text{V}}{0.1\ \text{m}} = 20\ \text{Vm}^{-1}$$

For silicon block :

$$n_h = n_e = n_i = 1.5 \times 10^{16} \text{m}^{-3}$$

$\therefore$ Electron current,

$$I_e = e n_e\, Av_e = e n_e\, A.\mu_e\, E \qquad \left[\because \mu_e = \frac{v_e}{E}\right]$$

$$= 1.6 \times 10^{-19} \times 1.5 \times 10^{16} \times 10^{-4} \times 0.135 \times 20\ \text{A}$$

$$= 6.48 \times 10^{-7}\ \text{A}$$

Hole current,

$$I_h = e n_h\, Av_h = e n_h\, A.\mu_h\, E \qquad \left[\because \mu_h = \frac{v_h}{E}\right]$$

$$= 1.6 \times 10^{-19} \times 1.5 \times 10^{16} \times 10^{-4} \times 0.048 \times 20\ \text{A}$$

$$= 2.304 \times 10^{-7}\ \text{A}$$

Total current,

$$I = I_e + I_h = (6.48 + 2.304) \times 10^{-7}\ \text{A}$$

$$= 8.78 \times 10^{-7}\ \text{A} = \mathbf{0.878\ \mu A}.$$

For germanium block :

$$n_h = n_e = n_i = 2.4 \times 10^{19}\ \text{m}^{-3}$$

$\therefore$ Electron current,

$$I_e = e n_e\, Av_e = e n_e\, A\mu_e\, E$$

$$= 1.6 \times 10^{-19} \times 2.4 \times 10^{19} \times 10^{-4} \times 0.39 \times 20\ \text{A}$$

$$= 2.995 \times 10^{-3}\ \text{A}$$

Hole current,

$$I_h = e n_h\, Av_h = e n_h\, A\mu_h\, E$$

$$= 1.6 \times 10^{-19} \times 2.4 \times 10^{19} \times 10^{-4} \times 0.19 \times 20\ \text{A}$$

$$= 1.495 \times 10^{-3}\ \text{A}$$

Total current,

$$I' = I_e + I_h$$

$$= (2.995 + 1.495) \times 10^{-3}\ \text{A}$$

$$= 4.454 \times 10^{-3}\ \text{A} = \mathbf{4.454\ mA}.$$

Example 10. *The resistivity of pure silicon is 3000 Ωm and the electron and hole mobilities are 0.12 $m^2\ V^{-1}s^{-1}$ and 0.045 $m^2\ V^{-1}s^{-1}$ respectively, determine (a) the resistivity of a specimen of the material when 10^{19} atoms of phosphorus are added per m^3, (b) the resistivity of the specimen if further 2×10^{19} boron atoms per m^3 are also added.*

Solution. The resistivity of pure silicon is given by

$$\rho = \frac{1}{\sigma} = \frac{1}{e n_i (\mu_e + \mu_h)}$$

$\therefore$ Intrinsic carrier concentration,

$$n_i = \frac{1}{e\rho(\mu_e + \mu_h)}$$

$$= \frac{1}{1.6\times10^{-19}\times3000\times(0.12+0.045)}\ m^{-3}$$

$$= 1.437\times10^{16}\,m^{-3}$$

(a) When 10^{19} donor atoms of phosphorus are added per m^3 :

$$n_e n_h = n_i^2 = (1.437\times10^{16})^2 = 2.066\times10^{32}$$

and $$n_e - n_h = N_d - N_a = 10^{19}$$

As $n_e >> n_h$, therefore, $n_e \simeq 10^{19}$

Hence $$\rho = \frac{1}{en_e\mu_e} = \frac{1}{1.6\times10^{-19}\times10^{19}\times0.12}$$

$$= \mathbf{5.21\ \Omega m}.$$

(b) When 2×10^{19} acceptor atoms of boron are further added :

$$n_h - n_e = N_a - N_d = 2\times10^{19} - 10^{19} = 10^{19}$$

As $n_h >> n_e$, therefore, $n_h \simeq 10^{19}$

Hence $$\rho = \frac{1}{en_h\mu_h} = \frac{1}{1.6\times10^{-19}\times10^{19}\times0.025}$$

$$= \mathbf{25\ \Omega m}.$$

Problems For Practice

1. Mobilities of electrons and holes in a sample of intrinsic germanium at room temperature are $0.54\ m^2V^{-1}s^{-1}$ and $0.18\ m^2V^{-1}s^{-1}$ respectively. If the electron and hole densities are equal to $3.6\times10^{19}\,m^{-3}$, calculate the germanium conductivity. **[BIT Ranchi 1997]**
(Ans. $4.147\ Sm^{-1}$)

2. A semiconductor has the electron concentration of $8\times10^{13}\,cm^{-3}$ and hole concentration of $4\times10^{13}\,cm^{-3}$. Is the semiconductor *p*-type or *n*-type ? Also calculate the resistivity of this semiconductor. Given electron mobility $= 24{,}000\ cm^2\ V^{-1}s^{-1}$ and hole mobility $= 200\ cm^2V^{-1}s^{-1}$. **[Punjab 01]**
(Ans. *n*-type, $3.254\times10^{-2}\Omega$ m)

3. A semiconductor has the electron concentration $4\times10^{12}\,cm^{-3}$ and the hole concentration $7\times10^{13}\,cm^{-3}$. Is the substance *n*-type or *p*-type ? Also calculate the conductivity of this semiconductor. Given electron mobility $= 2{,}2000\ cm^2\ V^{-1}s^{-1}$ and hole mobility $= 150\ cm^2\ V^{-1}s^{-1}$. **[Punjab 01]**
(Ans. *p*-type, $1.576\ Sm^{-1}$)

4. Determine the number density of donor atoms which have to be added to an intrinsic germanium to produce an *n*-type semiconductor of conductivity $0.06\ Sm^{-1}$. Given the mobility of electrons $= 0.39\ m^2V^{-1}s^{-1}$. Neglect the contribution of holes to the conductivity. (Ans. $96\times10^{16}\,m^{-3}$)

5. Germanium is doped one part per million with indium at room temperature. Calculate the conductivity of doped germanium. Given : concentration of Ge atoms $= 4.4\times10^{28}\,m^{-3}$, intrinsic carrier concentration $(n_i) = 2.4\times10^{19}\,m^{-3}$, $\mu_e = 0.39\ m^2V^{-1}s^{-1}$ and $\mu_h = 0.19\ m^2V^{-1}s^{-1}$.
(Ans. $1.34\times10^3\,ohm^{-1}m^{-1}$)

6. Determine the conductivity and resistivity of pure germanium at 300 K, assuming that at this temperature the concentration of germanium is $2.5\times10^{13}\,cm^{-3}$. The electron and hole mobilities are $3600\ cm^2\ V^{-1}s^{-1}$ and $1700\ cm^2V^{-1}s^{-1}$, respectively. (Ans. $2.12\ Sm^{-1}$, $0.472\ \Omega m$)

7. The resistivity of pure germanium at a particular temperature is $0.52\ \Omega m$. If the material is doped with 10^{20} atoms m^{-3} of a trivalent impurity material, determine the new resistivity. The electron and hole mobilities are given to be 0.2 and $0.4\ m^2V^{-1}s^{-1}$ respectively. (Ans. $0.195\ \Omega m$)

8. A sample of germanium is doped to the extent of 10^{14} donor atoms per cm^3 and 7×10^{13} acceptor atoms per cm^3. The resistivity of pure germanium at the temperature of the sample is $60\ \Omega$ cm. Find the total conduction current density due to an applied electric field of $2\ V\,cm^{-1}$. The electron and hole mobilities are given to be $3800\ cm^2V^{-1}s^{-1}$ and $1800\ cm^2V^{-1}s^{-1}$, respectively. (Ans. $52.3\ mA\ cm^{-2}$)

9. The energy gap in germanium is 0.75 eV. Compare the intrinsic conductivities of germanium at 300 K and 330 K. Take $k_B = 8.6\times10^{-5}eVK^{-1}$. (Ans. 3.74)

HINTS

1. Conductivity,
$\sigma = e(n_e\mu_e + n_h\mu_h) = en_i(\mu_e + \mu_h)$
$= 1.6\times10^{-19}\times3.6\times10^{19}(0.54+0.18) = \mathbf{4.147\ Sm^{-1}}$.
2. Proceed as in Example 7.
3. $\sigma = e(n_e\mu_e + n_h\mu_h)$
$= 1.6\times10^{-19}(4\times10^{12}\times22000 + 7\times10^{13}\times150)$
$= 1.576\times10^{-2}\ S\,cm^{-1} = \mathbf{1.576\ Sm^{-1}}$.
4. Use the relation, $n_e = \frac{\sigma}{e\mu_e}$
6. Take $n_e = n_h = n_i = 2.5\times10^{13}\,cm^{-3}$.
7. Resistivity of pure germanium,
$$\rho = \frac{1}{\sigma} = \frac{1}{en_i(\mu_e+\mu_h)}$$
$$\therefore\ n_i = \frac{1}{e\rho(\mu_e+\mu_h)} = \frac{1}{1.6\times10^{-19}\times0.52(0.2+0.4)}$$
$$= 2\times10^{19}\,m^{-3}$$

When 10^{20} acceptor atoms are further added,

$n_h - n_e = N_a - N_d = 10^{20} - 2 \times 10^{19} = 8 \times 10^{19}\ m^{-3}$

As $n_h > n_e$, so $n_h = 8 \times 10^{19}$

$$\therefore \quad \rho = \frac{1}{e n_h \mu_h} = \frac{1}{1.6 \times 10^{-19} \times 8 \times 10^{19} \times 0.4}$$

$$= 0.195\ \Omega\ m.$$

8. Total conduction current density is given by

$$J = \sigma E = e(\mu_e n_e + \mu_h n_h) E$$

9. Use the relation, $\sigma = \sigma_0 e^{-E_g/2k_B T}$.

14.17 *p-n* JUNCTION

21. *What is a p-n junction ? Explain with the help of a diagram, how is a depletion layer formed near its junction. How is a potential barrier set up in it ?*

p-n junction. *It is a single crystal of Ge or Si doped in such a manner that one half portion of it acts as p-type semiconductor and the other half as n-type semiconductor.* Here, the term junction implies the boundary or region of transition between *n*-type and *p*-type semiconductor materials.

A *p-n* junction cannot be made just by placing a *p*-type semiconductor in close contact with *n*-type semiconductor. The two separate semiconductors cannot have a *continuous contact* at the atomic level. The junction will behave as a discontinuity for the flowing charge carriers. So both acceptor and donor impurities must be grown in a single Si or Ge crystal.

A *p-n* junction is the key, to all semiconductor devices. For example, a *p-n* junction can be used as a rectifying diode. Another important device is a transistor which has *n-p-n* or *p-n-p* configuration.

A *p*-type or *n*-type silicon crystal can be obtained by adding suitable acceptor or donor-impurity into silicon melt while growing a crystal. These crystals are cut into thin slices called ***wafers***. Semiconductor devices are usually made on these wafers.

Unbiased *p-n* junction : Depletion region and potential barrier in a *p-n* junction. Two important processes involved during the formation of *p-n* junction are *diffusion* and *drift*. When a *p-n* junction is formed, the *p*-side of the junction has a higher concentration of holes while the *n*-side has a higher concentration of electrons. Due to the concentration gradient at the junction, holes begin to diffuse from *p*-side to *n*-side ($p \rightarrow n$) and electrons begin to diffuse from *n*-side to *p*-side ($n \rightarrow p$). As holes diffuse from $p \rightarrow n$ side, they leave behind –ve acceptor ions which set up a layer of negative charge or negative *space-charge region* on the *p*-side of the junction. Similarly, as the electrons diffuse from $n \rightarrow p$ side, they leave behind +ve donor ions which set up a layer of positive charge or *positive space-charge region* on the *n*-side of the junction. This sets up an electric field near the junction from $n \rightarrow p$ side. Any hole near the junction is pushed towards *n*-side. Similarly, any conduction electron near the junction is pushed by the electric field towards the *p*-side. Consequently, no charge carriers are left in a small region near the junction as shown in Fig. 14.13(*a*). *The small region in the vicinity of the junction which is depleted of free charge carriers and has only immobile ions is called* **depletion region**.

The distribution of charge near the junction is shown in Fig. 14.13(*b*). *The accumulation of negative charges in the p-region and positive charges in the n-region sets up a potential difference across the junction. This acts as a barrier and is called* **barrier potential** V_B [Fig. 14.13(*c*)] which opposes the further diffusion of electrons and holes across the junction. Only those electrons and holes which have energy atleast eV_B are able to cross this barrier and some diffusion takes place. *This diffusion of majority charge carriers across the junction gives rise to an electric current from $p \rightarrow n$ side and is called* **diffusion current.**

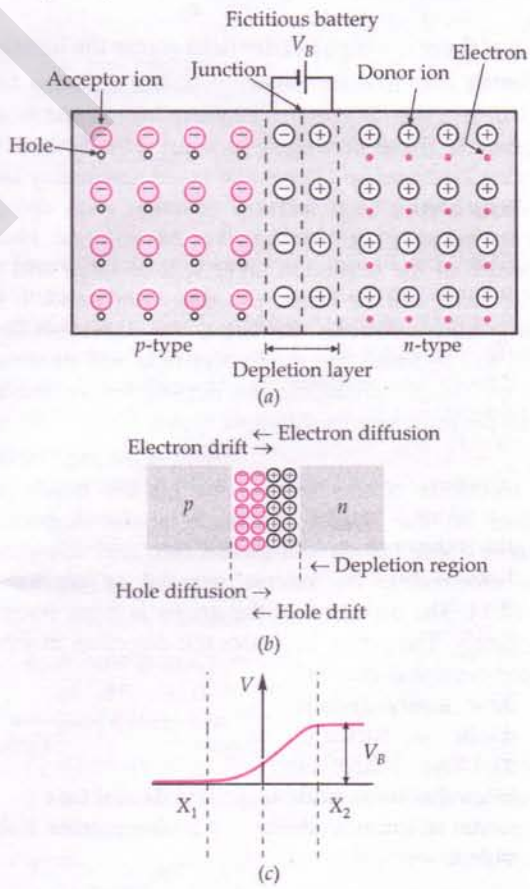


Fig. 14.13. Formation of *p-n* junction : (*a*) depletion layer consisting of immobile –ve and +ve ions (*b*) diffusion and drift currents (*c*) barrier potential.

The barrier potential V_B sets up a *barrier field* $\vec{E}_B$ *in the direction* $n \rightarrow p$ *side.*

In the depletion region, electron-hole pairs are continuously produced due to thermal or electric field conditions. The electric field $\vec{E}_B$ immediately pushes the electrons towards the *n*-side and holes towards the *p*-side. *This current set up by the barrier field from* $n \rightarrow p$ *side is called* **drift current**.

The drift current and diffusion current are in opposite directions. In equilibrium state, the diffusion current is equal to the drift current and there is no net flow of charge across the junction.

The barrier potential V_B depends on (*i*) the nature of the semiconductor, (*ii*) temperature, and (*iii*) the amount of doping. The value of barrier potential is 0.7 V for Si and 0.3 V for Ge semiconductors.

If barrier potential, $V_B \simeq 0.5$ V

depletion width, $d \simeq 1\,\mu = 10^{-6}$ m

then, electric field, $E_B \simeq \dfrac{0.5 \text{ V}}{10^{-6} \text{ m}} = 5 \times 10^5 \text{ Vm}^{-1}$

Thus there is a high barrier field across the junction.

Let us see how *the barrier field and depletion layer width depend on the doping concentrations in the n- and p-regions.* If these concentrations are small, then the diffusing electrons and holes will cover reasonably large distances before they suffer a collision with another hole or electron to get annihated or recombined. Hence the width of the depletion layer will be large and the barrier field will be weak. On the other hand, if the doping concentrations are large, the depletion layer width will be small and the barrier field will be strong. Thus by simply changing the doping levels, we can obtain *p-n* junctions of different types.

Circuit symbol for a p-n junction. A *p-n* junction has two electrode connections – one on the *p*-side and another on the *n*-side. Hence it is also known as ***junction diode*** (diode : di-means two and ode comes from electrode). Its circuit symbol is shown in Fig. 14.14. The direction of the arrow is from *p*-region to *n*-region. The arrow indicates the direction in which the conventional current can flow easily (when the diode is forward biased). The *p*-side is known as the *anode* and the *n*-side is known as the *cathode*.

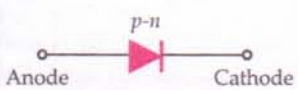


Fig. 14.14 Symbol for a *p-n* junction diode.

14.18 WORKING OF A *p-n* JUNCTION

22. *Explain the working of a junction diode when it is (i) forward biased and (ii) reverse biased.*

Working of a *p-n* junction. An external potential difference can be applied to a *p-n* junction in two ways :

1. Forward biasing. *If the positive terminal of a battery is connected to the p-side and the negative terminal to the n-side, then the p-n junction is said to be forward biased.*

As shown in Fig. 14.15(*a*), here the applied voltage V opposes the barrier voltage V_B. As a result of this

(*i*) the effective barrier potential decreases to $(V_B - V)$ and hence the energy barrier across the junction decreases, as shown in Fig. 14.15(*b*),

(*ii*) the majority charge carries *i.e.*, holes from *p*-side and electrons from *n*-side begin to flow towards the junction,

(*iii*) the diffusion of electrons and holes into the depletion layer decreases its width, and

(*iv*) the effective resistance across the *p-n* junction decreases.

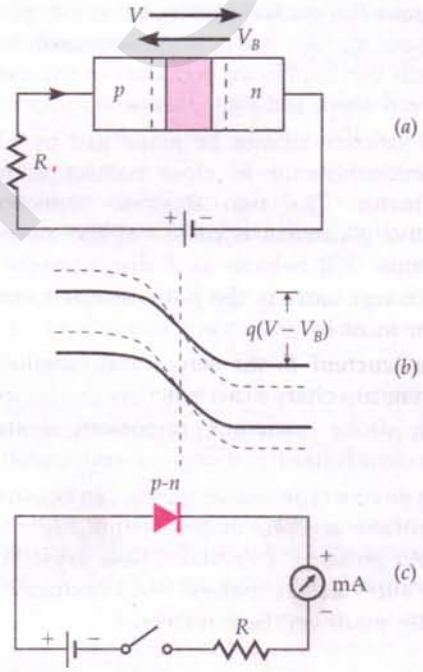


Fig. 14.15 (*a*) Reduced depletion layer, (*b*) Reduced energy barrier, (*c*) Symbolic representation, for a forward biased *p-n* junction.

When V exceeds V_B, the majority charge carriers start flowing easily across the junction and set up a large current (≈ mA), called forward *current*, in the circuit. The current increases with the increase in applied voltage.

2. Reverse biasing. *If the positive terminal of a battery is connected to the n-side and negative terminal to the p-side, then the p-n junction is said to be reverse biased.*

As shown in Fig. 14.16(*a*), the applied voltage V and the barrier potential V_B are in the same direction.

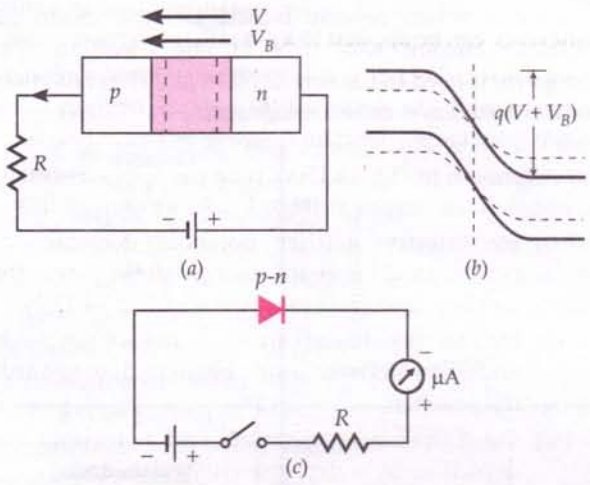


Fig. 14.16 (*a*) Increased depletion layer, (*b*) Increased energy barrier, (*c*) Symbolic representation for a reverse biased *p-n* junction.

As a result of this

(*i*) the barrier potential increases to $(V_B + V)$ and hence the energy barrier across the junction increases,

(*ii*) the majority charge carriers move away from the junction, increasing the width of the depletion layer,

(*iii*) the resistance of the *p-n* junction becomes very large, and

(*iv*) no current flows across the junction due to majority charge carriers.

However, at room temperature there are always present some minority charge carriers like holes in *n*-region and electrons in *p*-region. The reverse biasing pushes them towards junction, setting a current, called *reverse or leakage current*, in the external circuit in the opposite direction. As the minority charge carriers are much less in number than the majority charge carriers, hence the reverse current is small (≈ μA).

14.19 *V-I* CHARACTERISTICS OF A *p-n* JUNCTION DIODE

23. *With the help of suitable circuit diagrams, explain how will you sketch the characteristic curves of a junction diode. Sketch and explain these curves.*

V-I characteristics of a p-n junction diode. A graph showing the variation of current flowing through a p-n junction with the voltage applied across it (both when it is forward and reverse biased) *is called the* ***voltage-current*** *or* ***V-I characteristic*** *of a p-n* junction

1. Forward bias characteristic. Fig. 14.17 shows the experimental arrangement for studying the characteristic curve of a *p-n* junction when it is ***forward biased.*** A battery is connected across the *p-n* junction diode through a potentiometer (or rheostat) so that the voltage applied to the diode can be changed. The milliammeter measures the current through the diode and the voltmeter measures the voltage across the diode. For different values of voltages, the value of current is noted. A graph is plotted between *V* and *I*, as shown in Fig. 14.18. This voltage-current graph is called ***forward characteristic.***

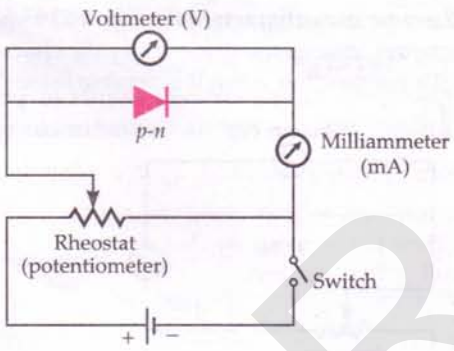


Fig. 14.17 Circuit for studying *V-I* characteristic of a forward biased diode.

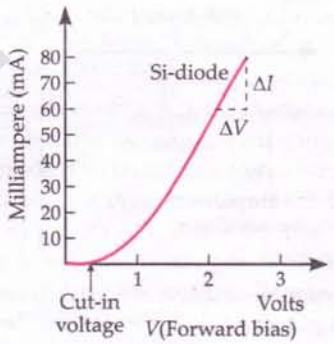


Fig. 14.18 Forward characteristic of a junction diode.

Important features of the graph. (*i*) The *V-I* graph is not a straight line *i.e.*, a junction diode does not obey *Ohm's law.*

(*ii*) Initially, the current increases very slowly almost negligibly, till the voltage across the diode crosses a certain value, called the ***threshold-voltage*** or ***cut-in voltage***. The value of the cut-in voltage is about 0.2 V for a Ge diode and 0.7 V for a Si diode. Before this characteristic voltage, the depletion layer plays a dominant role in controlling the motion of charge carriers.

(*iii*) After the cut-in voltage, the diode current increases rapidly (exponentially), even for a very small increase in the diode bias voltage. Here the majority charge carriers feel negligible resistance at the junction *i.e.*, the resistance across the junction is quite low.

2. Reverse bias characteristic. Fig. 14.19 shows the experimental arrangement for studying characteristic curve of a *p-n* junction when it is reverse biased. Here a

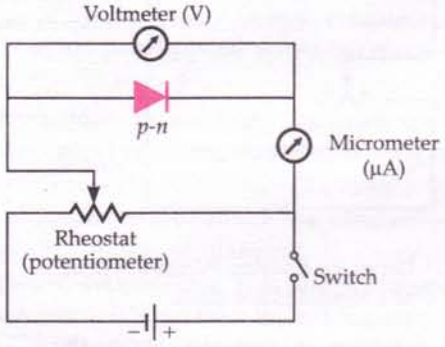


Fig. 14.19 Circuit for studying *V-I* characteristic of a reverse biased diode.

microammeter is used to measure the small currents through the reverse biased diode. A *V-I* graph of the type shown in Fig. 14.20 is obtained. It is called ***reverse characteristic*** of the junction diode.

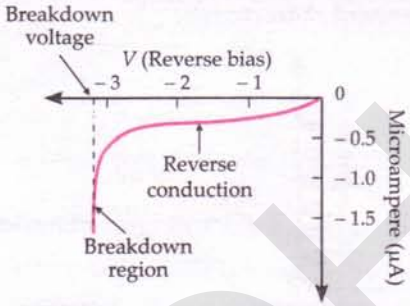


Fig. 14.20 Reverse characteristic of a junction diode.

Important features of the graph. (*i*) When the diode is reverse biased, the reverse bias voltage produces a very small current, about a few microamperes which almost remains constant with bias. This small current is called ***reverse saturation current***. It is due to the drift of minority charge carriers (a few holes in *n*-region and a few electrons in *p*-region) across the junction.

(*ii*) When the reverse voltage across the *p-n* junction reaches a sufficiently high value, the reverse current suddenly increases to a large value. This voltage at which breakdown of the junction diode occurs is called ***Zener breakdown voltage*** or ***peak-inverse voltage*** of the diode. It ranges from as low as 1 to 2 V to several hundred volts, depending on the dopant density and the depletion layer.

Fig. 14.21 shows the complete *V-I* characteristic of a *p-n* junction. Obviously, it is a *unidirectional current* characteristic. A junction diode offers a very small resistance when forward biased and has a very large resistance when reverse biased *i.e.*, the diode can conduct current well only in one direction. This property is used to convert a.c. into d.c. The conversion of a.c. into d.c. is called *rectification*.

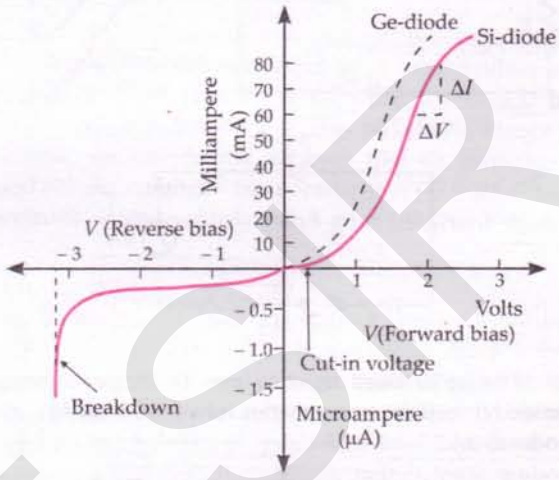


Fig. 14.21 Complete *V-I* characteristic of a junction diode.

14.20 DYNAMIC RESISTANCE OF A JUNCTION DIODE

24. *Define dynamic resistance of a junction diode.*

Dynamic resistance of a junction diode. The current- voltage graph of junction diode is *non-linear, i.e.,* Ohm's law is not obeyed. The resistance of the junction diode varies with the applied voltage. In such cases, it is useful to define a quantity called ***dynamic*** *or* ***ac-resistance*** of the diode. *It is the ratio of the small change in applied voltage* ΔV *to the corresponding change in current* ΔI. It is given by

$$r_d = \frac{\Delta V}{\Delta I}$$

Above the threshold voltage, the diode characteristic is *linear*. In the linear region, r_d *is almost independent of V* and Ohm's law is obeyed.

14.21 JUNCTION DIODE AS A RECTIFIER

25. *What is a rectifier ? What is the principle of a rectifier ?*

Rectifier. *The process of converting alternating current into direct current is called* ***rectification*** *and the device used for this process is called* ***rectifier.***

Principle of a rectifier. When a *p-n* junction diode is forward biased, it offers less resistance and a current flows through it ; but when it is reverse biased, it offers high resistance and almost no current flows through it. This unidirectional property of a diode enables it to be used as a rectifier. When *a.c.* signal is fed to a diode, the diode is forward biased during the positive half cycle

and a current flows through it. During the negative half cycle, the diode is reverse biased and it does not conduct. Thus the signal is rectified.

The *p-n* junctions can be used as

(*i*) *a half-wave rectifier,* and

(*ii*) *a full-wave rectifier.*

14.22 JUNCTION DIODE AS A HALF-WAVE RECTIFIER

26. *With the help of a circuit diagram, explain the use of a junction diode as a half-wave rectifier. Draw the input and output waveforms.*

Junction diode as a half-wave rectifier. A half-wave rectifier consists of a transformer, a junction diode D and a load resistance R_L. The primary coil of the transformer is connected to the a.c. mains and the secondary coil is connected in series with the junction diode D and load resistance R_L. We assume that the diode is ideal so that it offers infinite resistance during the reverse biasing.

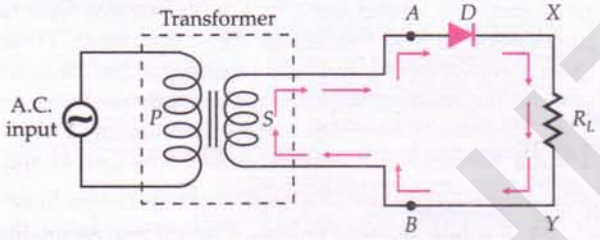


Fig. 14.22 Half-wave rectifier circuit.

Working. When a.c. is supplied to the primary, the secondary of the transformer supplies desired alternating voltage across A and B. During the positive half cycle of a.c., the end A is positive and the end B is negative. The diode D is forward biased and a current I flows through R_L. As the input voltage increases or decreases, the current I also increases or decreases and so does output voltage ($= IR_L$) across the load R_L. Output voltage across R_L is of same waveform as the positive half wave of the input. During the negative half cycle, the end A becomes negative and B positive. The diode is reverse biased and no current flows. No voltage appears across R_L. In the next positive half cycle, again we get output voltage. The output voltage is unidirectional but pulsating, as shown in Fig. 14.23. Since the voltage across the load appears only during the positive half cycle of the input *a.c.*, this process is called ***half-wave rectification*** and the arrangement used is called a ***half-wave rectifier.***

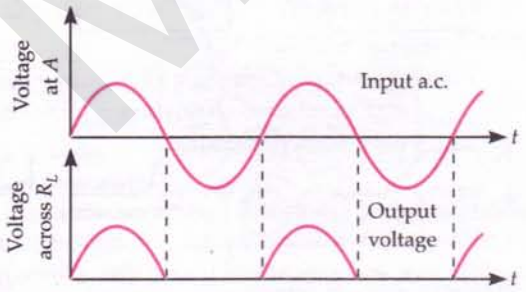


Fig. 14.23 Waveforms of input a.c. and output voltage obtained from a half-wave rectifier.

14.23 JUNCTION DIODE AS A FULL WAVE RECTIFIER

27. *With the help of a circuit diagram, explain full wave rectification using junction diodes. Draw the waveforms of input and output voltages.*

Junction diode as a full wave rectifier. A full wave rectifier consists of a transformer, two junction diodes D_1 and D_2 and a load resistance R_L. The input *a.c.* signal is fed to the primary coil P of the transformer. The two ends A and B of the secondary S are connected to the *p*-ends of diodes D_1 and D_2. The secondary is tapped at its central point T which is connected to the *n*-ends of the two diodes through the load resistance R_L, as shown in Fig. 14.24.

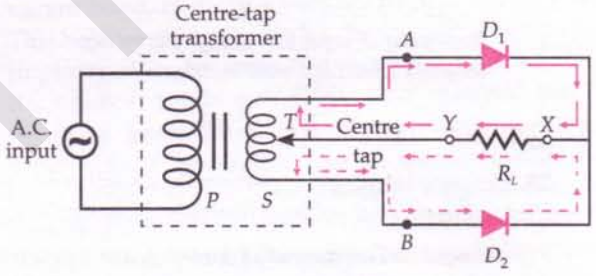


Fig. 14.24 Full wave rectifier circuit.

Working. At any instant, the voltages at the end A (input of D_1) and end B (input of D_2) of the secondary with respect to the centre tap T will be out of phase with each other. Suppose during the positive half cycle of a.c. input, the end A is positive and the end B is negative with respect to the centre tap T. Then the diode D_1 gets forward biased and conducts current along the path AD_1XYTA, as indicated by the solid arrows. The diode D_2 is reverse biased and does not conduct. During the negative half cycle, the end A becomes negative and the end B becomes positive with respect to the centre tap T. The diode D_1 gets reverse biased and does not conduct. The diode D_2 conducts current along the path BD_2XYTB, as indicated by broken arrows. As during both half cycles of input a.c. the current through load R_L flows in the same direction ($X \rightarrow Y$), so we get a pulsating d.c.

voltage across R_L, as shown in Fig. 14.25. Since output voltage across the load resistance R_L is obtained for both half cycles of input a.c., this process is called ***full wave rectification*** and the arrangement used is called ***full-wave rectifier.***

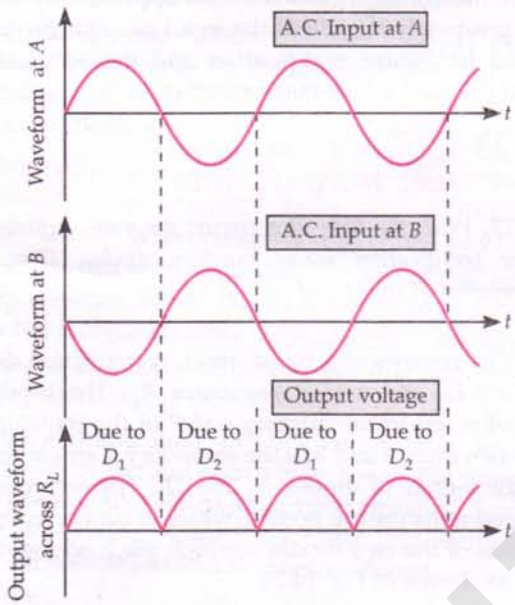


Fig. 14.25 Waveforms of input a.c. and output voltage obtained from a full wave rectifier.

14.24 FILTER CIRCUITS

28. *Describe simple filter circuits for smoothening the rectified voltages obtained from junction diode rectifiers.*

Filter circuits. The output obtained from a junction diode rectifier is unidirectional but pulsating. Such a signal can be considered as the sum of a d.c. signal superimposed with many a.c. signals of different harmonic frequencies. We can obtain d.c. voltage by filtering out the a.c. components. We describe here two simplest filter circuits.

1. Series inductor filter. Figure 14.26 shows the circuit of a full wave rectifier with an inductor of inductance L connected in series with its load resistance R_L.

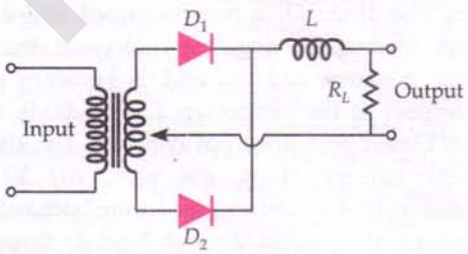


Fig. 14.26 Full wave rectifier with series inductor filter.

The inductance L offers a reactance $X_L = 2\pi f L$ to the flow of current through it. Clearly, it blocks high frequency a.c. component and allows low frequency d.c. component to pass through it. A smooth d.c. voltage appears across the load resistance.

2. Shunt capacitor filter. Figure 14.27 shows the circuit of a full wave rectifier with a capacitor of capacitance C connected in parallel with its load resistance R_L.

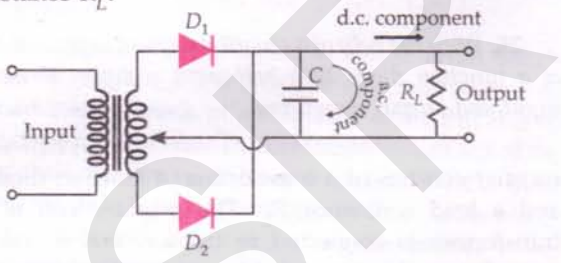


Fig. 14.27 Full wave rectifier with shunt capacitor filter.

The capacitor has a reactance of $X_C = 1/2\pi f C$. A high capacitance C offers a low impedance path to high frequency a.c. component but high, almost infinite, impedance to low frequency d.c. component. Hence the a.c. component is bypassed through C or filtered. A smooth d.c. voltage appears at the load resistance.

14.25 CAUSE OF REVERSE BREAKDOWN OF A JUNCTION DIODE

29. *Explain the two processes which are responsible for the breakdown of a junction diode.*

Cause of reverse breakdown of a junction diode. The breakdown of a junction diode may occur through two different processes :

1. Zener breakdown. This process occurs in *heavily doped* junction diodes. Fig. 14.28(*a*) shows a *p-n* junction in which the symbols p^+ and n^+ indicate that

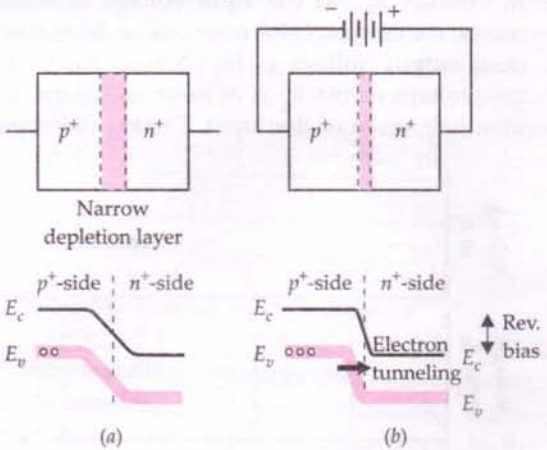


Fig. 14.28 (*a*) Unbiased p^+–n^+ and (*b*) reverse biased p^+–n^+ junctions of a Zener diode.

both p- and n-sides are heavily doped by acceptor and donor impurities respectively. Due to high dopant density, the width of the junction layer is small and the barrier field ($E = V / d$) is high.

When a large reverse bias is applied across such a diode, the depletion layer and the energy bands get modified, as shown in Fig. 14.28(b). As the depletion width is very small ($< 10^{-7}$ m), even a small voltage (say 4 V) will set up a high electric field of 4×10^7 Vm^{-1}. This high electric field strips off many electrons from valence band which tunnel to the n-side through the thin depletion layer. This method of emission of electrons beyond a certain reverse bias voltage V_Z is called *internal field emission*. It gives rise to a large reverse current or breakdown current, as shown in Fig. 14.29. *This breakdown in a diode due to the band-to-band tunneling is called* ***Zener breakdown*** and such diode is called ***Zener diode***. Here the breakdown voltage is of the order of few volts.

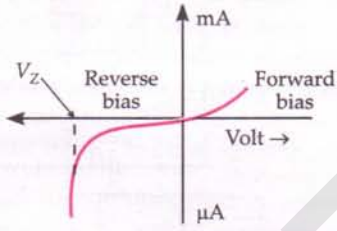


Fig. 14.29 *V-I* characteristic of a Zener diode.

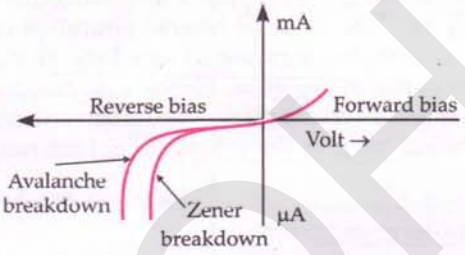


Fig. 14.30 *V-I* characteristic-curve for an avalanche diode.

2. Avalanche breakdown. This process occurs in diodes having low level of doping and hence wide depletion layer. When the reverse bias voltage is sufficiently high, the minority charge carriers get highly accelerated. Their kinetic energy becomes high enough and they *knock-off* electrons from the covalent bonds of the semiconductor. The newly generated electron-hole pairs also get accelerated and cause ionisation. Thus a chain of collisions is set up which gives rise to a very large number of charge carriers. This leads to a large reverse current, as shown in Fig. 14.30. This phenomenon is called ***Avalanche breakdown*** and the device is called ***Avalanche diode***.

14.26 ZENER DIODE AS A VOLTAGE REGULATOR

30. *What is a Zener diode ? Give its symbol. Explain its use as a voltage regulator.*

Zener diode. *A junction diode specially designed to operate only in the reverse breakdown region continuously (without getting damaged) is called a Zener diode.* Zener diodes with different breakdown voltages can be obtained by changing the doping concentrations of p- and n-sides which, in turn, change the width of depletion layer and also the barrier field across the junction. The symbol of a Zener diode is shown in Fig. 14.31.

Fig. 14.31 Symbol for Zener diode.

Zener diode as a voltage regulator : Principle. *When a Zener diode is operated in the reverse breakdown region, the voltage across it remains practically constant (equal to the breakdown voltage V_Z) for a large change in the reverse current.* The use of Zener diode as a d.c. voltage regulator is based on this fact.

Working. Figure 14.32 shows the circuit for using Zener diode as a voltage regulator. Here the Zener diode is connected in reverse bias to a source of fluctuating *d.c.* (*e.g.*, the output from a rectifier) through a *dropping resistor* R_S. Thus the voltage gets divided between R_S and zener diode. The output is obtained across the load resistance R_L, connected in parallel with the zener diode.

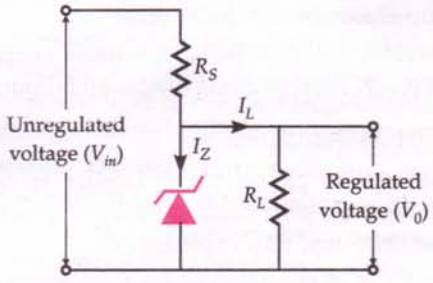


Fig. 14.32 Zener diode as a voltage regulator.

If the input voltage increases, the current through R_S and Zener diode also increases. This increases the voltage drop across R_S without any change in the voltage across the Zener diode. This is because in the breakdown region, Zener voltage remains constant even though the current through the Zener diode changes. Similarly, if the input voltage decreases, the voltage across R_S decreases without any change in the voltage across the Zener diode. Thus any increase/decrease of the input voltage results in, increase/decrease of the voltage drop across R_S without any change in voltage across Zener diode. Hence the Zener diode acts as a voltage regulator.

Figure 14.33 shows the graph of output voltage V_0 versus input voltage V_{in} for a Zener diode. Clearly, the output voltage remains constant after the reverse breakdown voltage V_Z.

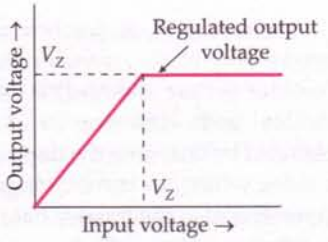


Fig. 14.33 Graph of V_0 versus V_{in} for a Zener diode.

14.27 PHOTONIC *p-n* JUNCTION DEVICES

31. *What are photonic p-n junction devices ? How are they classified ?*

Photonic *p-n* junction devices. *The p-n junctions can be designed so that current through them changes either by causing electron excitation (from valence band to the conduction band) by light photons, or conversely through electron excitation by a suitable bias voltage resulting in the emission of light photons. These semiconducting devices are called* ***photonic*** *or* ***opto-electronic devices***. In such devices, light photons play an important role in the overall functioning of the device.

The photonic *p-n* junction devices can be classified as follows :

(*i*) *Photo-detectors* used for detecting light signals *e.g.*, photodiodes and photoconducting cell.

(*ii*) *Photovoltaic devices* which convert light energy into electricity *e.g.*, solar cells.

(*iii*) Devices for converting electrical energy into light *e.g.*, light emitting diodes and diode lasers.

14.28 PHOTODIODES

32. *What is a photodiode ? Explain its working principle. Why is a photodiode operated in reverse bias ? Give some important uses of photodiodes.*

Photodiode. *A photodiode is a p-n junction fabricated from a photosensitive semiconductor and provided with a transparent window so as allow light to fall on its junction.* Its symbolic representation is shown in Fig. 14.34.

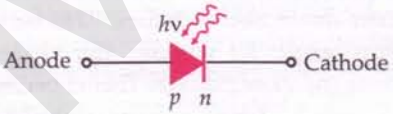


Fig. 14.34 Symbolic representation of a photodiode.

As shown in Fig. 14.35, a resistance R is connected in series with a reverse biased photodiode. The voltage is kept slightly less than the breakdown voltage. When no light is incident on the junction, a small reverse saturation current flows through the junction. This reverse current is due to thermally generated electron-hole pairs and is called *dark current*.

When the photodiode is illuminated with light photons of energy $h\nu$ greater than the energy gap E_g of the semiconductor, additional electron-hole pairs are generated due to the absorption of photons. This generation of photogenerated charge carriers occurs in or near the depletion region. Due to the junction field, electrons get collected on *n*-side and holes on the *p*-side setting up an emf. This sends a current through the load. In a reverse biased photodiode, we can easily observe the change in photocurrent with the change in radiation intensity. Hence a photodiode can be used to detect optical signals.

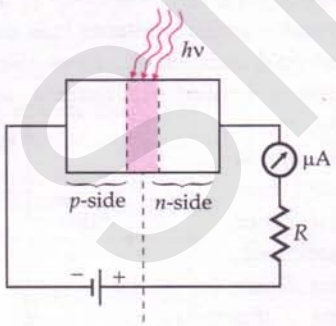


Fig. 14.35 A reverse biased photodiode illuminated with light.

When a photodiode is illuminated with light photons of energy $h\nu > E_g$, and increasing intensities I_1, I_2, I_3, etc., the value of reverse saturation current increases with the increase in intensity of incident light, as shown in Fig. 14.36. Hence, a measurement of the change in the reverse saturation current on illumination can give the values of light intensity.

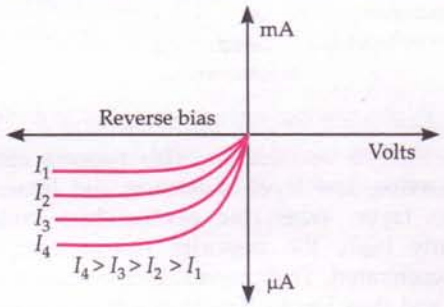


Fig. 14.36 Reverse bias currents through a photodiode when illuminated with different intensities.

A photodiode is preferably operated in reverse bias condition. Consider an *n*-type semiconductor. Its majority carrier (electron) density is much larger than the minority hole density *i.e.*, $n >> p$. When illuminated with light, both types of carriers increase equally in number.

$$n' = n + \Delta n \; ; \qquad p' = p + \Delta p$$

Now $n >> p$ and $\Delta n = \Delta p$

$$\therefore \quad \frac{\Delta n}{n} << \frac{\Delta p}{p}$$

That is, the fractional increase in majority carriers is much less than the fractional increase in minority carriers. Consequently, the fractional change due to the photo-effects on the minority carrier dominated reverse bias current is more easily measurable than the fractional change in the majority carrier dominated forward bias current. Hence, photodiodes are preferable used in the reverse bias condition for measuring light intensity.

Uses of photodiodes. A photodiode can turn its current ON and OFF in nanoseconds. So it can be used as a fastest photo-detector. The photodiodes are used for following purposes :

1. In detection of optical signals.
2. In demodulation of optical signals.
3. In light-operated switches.
4. In speed reading of computer punched cards.
5. In electronic counters.

14.29 LIGHT EMITTING DIODE

33. *What is a light emitting diode ? Draw a circuit diagram and explain its action. How do we choose the semiconductor, to be used in these diodes, if the emitted radiation, is to be in the visible region ? Give advantages of LEDs over conventional incandescent lamps.*

Light emitting diode (LED). *It is a heavily-doped forward-biased p-n junction which spontaneously converts the biasing electrical energy into optical energy, like infrared and visible light.*

LED is represented by either of the two symbols shown in Fig. 14.37(*a*). Its actual shape is also shown, the shorter lead responds to *n* - or cathode side while the longer lead corresponds to *p* - or anode side.

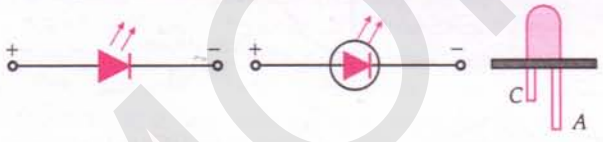


Fig. 14.37(*a*) LED symbol and shape.

A *p-n* junction made from a translucent semiconductor like gallium arsenide or indium phosphide is provided with metallised contacts, as shown in Fig. 14.37(*b*). When it is forward biased through a series resistance *R*, light photons are emitted from the non-metallised surface of the *n*-region. The series resistance *R* limits the current through the LED and hence controls the intensity of light emitted by it.

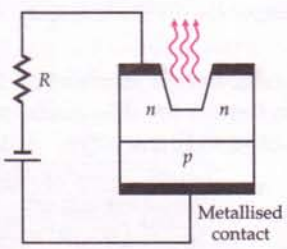


Fig. 14.37(*b*) A forward biased LED.

When the *p-n* junction is forward biased, electrons are sent from *n*-region → *p*-region (where they are minority carriers) and holes are sent from *p*-region → *n*-region (where they are minority carriers). Near the junction, the concentration of minority carriers increases as compared to the equilibrium concentration (*i.e.*, when there is no bias). On either side near junction, the excess minority carriers combine with the majority carriers. On recombination, the energy is released in the form of photons. Photons with energy equal to or slightly less than the band gap are emitted. When the forward bias of the diode is small, the intensity of emitted light is small. As the forward current increases, intensity of light increases and reaches a maximum. Further increase in forward current decreases the light intensity. LEDs are biased such that the light emitting efficiency is maximum.

The general shape of the *I-V* characteristics of an LED is similar to that of a normal *p-n* junction diode, as shown in Fig. 14.38. However, the barrier potentials are much higher and slightly different for each colour.

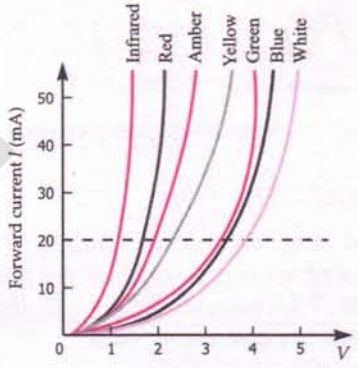


Fig. 14.38 *I-V* characteristics of LED.

Two important features of LEDs are :

1. The colour of light emitted by an LED depends on its band-gap energy.
2. The intensity of light emitted is determined by the forward current conducted by the *p-n* junction.

Choice of the semiconductor material used in LED. The wavelength of visible light ranges from 0.4 μm to 0.7 μm (energy from 3 eV to 1.8 eV). For a semiconductor to emit visible light, the minimum band gap must be 1.8 eV. The compound semiconductor Gallium – Arsenide – Phosphide ($GaAs_{1-x}P_x$) is used for making LEDs of different colours.

$GaAs_{0.6}P_{0.4}$ ($E_g \approx 1.9$ eV) is used for red LED.

GaAs ($E_g \approx 1.4$ eV) is used for infrared LED.

Advantages of LEDs over conventional incandescent lamps :

1. Low operational voltage and less power consumption.

2. Fast action and no warm up time required.
3. The bandwidth of emitted light is 100 Å to 500 Å *i.e.*, the light is nearly monochromatic.
4. Long life and ruggedness.
5. Fast ON/OFF switching capability.

Uses of LEDs :

1. Infrared LEDs are used in burglar-alarm systems.
2. In optical communication.
3. In image scanning circuits for picture phones.
4. LEDs are used as indicator lamps in radio receivers and other electronic equipment.
5. Hand calculators, cash registers, digital clocks, etc. use *seven-segment* red or green displays. Each segment is an LED and depending on which segment is energised, the display lights up the numbers 0 to 9, as shown in Fig. 14.39.

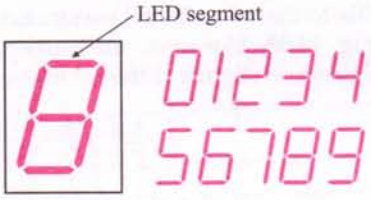


Fig. 14.39 Seven-segment display, each segment is an LED.

14.30 SOLAR CELL

34. *What is a solar cell ? Briefly describe the construction and working of a typical p-n junction solar cell. Give its V-I characteristic. Name the materials commonly used to prepare solar cells.*

Solar cell. *It is a junction diode which converts solar energy into electricity and is based on photovoltaic effect* (generation of voltage due to bombardment of light photons).

Construction. It consists of a *p-n* junction made from Si or GaAs. Here a thin layer of *p*-type is grown (by diffusion of a suitable acceptor impurity or by vapour deposition) on an *n*-type semiconductor. The top of the *p*-layer is provided with few finger electrodes. This leaves open enough space for the light to reach the thin *p*-layer and hence the underlying *p-n* junction. The bottom of the *n*-layer is provided with a current collecting electrode.

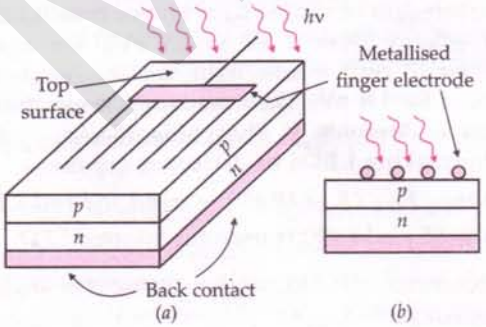


Fig. 14.40 (*a*) A typical *p-n* junction solar cell. (*b*) Sectional view of the solar cell.

Working. When light photons (with energy $h\nu > E_g$) reach the junction, they excite electrons from the valence band to conduction band, leaving behind equal number of holes in the valence band. These electron-hole pairs generated in the depletion region move in opposite directions due to the barrier field. Photo-generated electrons move towards *n*-sides and holes towards *p*-side. The collection of these charge carriers makes *p*-side a positive electrode and *n*-side a negative electrode. Hence ***photo-voltage*** is set up across the junction. When a load resistance R_L is connected in the external circuit, a photo-current I_L flows, as shown in Fig. 14.41(*a*). This current is proportional to the intensity of illumination.

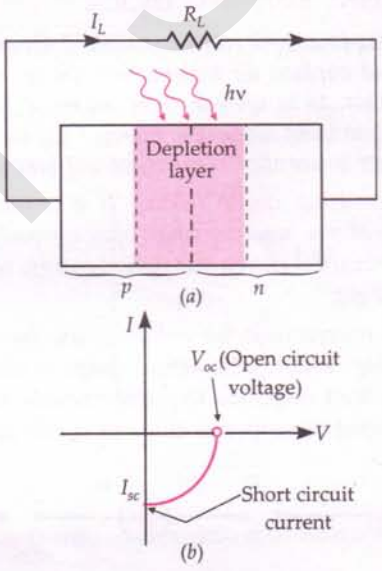


Fig. 14.41 (*a*) Photo-current through an illuminated *p-n* junction. (*b*) *V-I* characteristic of a solar cell.

Figure 14.41(*b*) shows the *V-I* characteristic of a solar cell. The open circuit voltage V_{OC} depends on the illumination. Hence the output power of a solar cell depends on the intensity of incident sunlight.

Materials used in the fabrication of solar cells. The semiconductors with band gap close to 1.5 eV are ideal materials for this purpose. Solar cells are made with semiconductors like

Si	(E_g = 1.1 eV),
GaAs	(E_g = 1.43 eV),
CdTe	(E_g = 1.45 eV),
$CuInSe_2$	(E_g = 1.04 eV), etc.

The important criteria for the selection of a material for solar cell fabrication are :

(*i*) Band gap (from 1.0 eV to 1.8 eV).
(*ii*) High optical absorption ($\sim 10^4 cm^{-1}$).
(*iii*) Electrical conductivity.
(*iv*) Availability of the raw material.
(*v*) Cost factor.

The *advantages* of solar cells are :

(*i*) pollution free,
(*ii*) long lasting, and
(*iii*) maintenance free.

They can be used anywhere as a self-generating source of electricity. But solar cells have high cost of installation and low efficiency.

Uses of solar cells :

1. We can use solar cells to charge storage batteries in day time and use the batteries for power during nights.
2. Solar cells, or better called photocells, are used in light meters in photography.
3. Some wrist watches and hand calculators are powered by solar cells.
4. Spacecrafts make use of arrays of solar cells or solar panels to provide electrical energy.

14.31 ADVANTAGES OF SEMICONDUCTOR DIODES OVER VACUUM DIODES

35. *Give some advantages and disadvantages of semiconductor diodes over vacuum diodes.*

Advantages of semiconductor diodes over vacuum diodes :

1. No cathode heating is required in a junction diode for the production of charge carriers.
2. A *p-n* junction diode is much smaller in size, robust and compact and hence easy to handle.
3. It starts operating as soon as it is switched on.
4. It can be used for much higher frequencies.
5. It dissipates less heat and is highly efficient in operation.
6. It has much longer life.
7. Voltage drop across a junction diode is very small compared to that across a vacuum diode.
8. No vacuum has to be created for its operation.

Disadvantage. It is highly sensitive to temperature and gets burnt up even if a moderately high current is passed through it.

Examples based on p-n Junction

Formulae Used

1. The d.c. resistance of a junction diode, $r_{dc} = \frac{V}{I}$
2. The dynamic or a.c. resistance of a junction diode,
   r_d or $r_{ac} = \frac{\Delta V}{\Delta I}$
3. Voltage equation for a diode circuit,
   Applied voltage, $V = V_d + IR$
4. For a Zener diode, $V_Z = V_i - RI$
   Series resistor, $R = \frac{V_i - V_Z}{R}$
5. Average value of d.c. obtained from a half-wave rectifier, $I_{dc} = \frac{I_o}{\pi}$.
6. Average value of d.c. obtained from a full-wave rectifier, $I_{dc} = \frac{2I_o}{\pi}$.

Units Used

Voltage is in volt, current in ampere and resistance in ohm.

Example 11. *Figure* 14.42 *shows the characteristic curve of a junction diode. Determine the d.c. and a.c. resistance of the diode, when it operates at* 0.3 *V.*

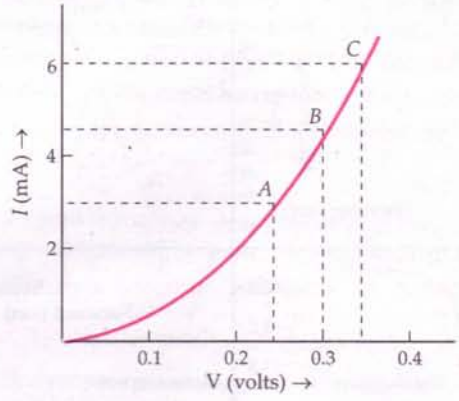


Fig. 14.42

Solution. The d.c. resistance is just equal to the voltage divided by current.

$$\therefore \quad r_{dc} = \frac{V_B}{I_B} = \frac{0.3 \text{ V}}{4.5 \times 10^{-3} A} = \mathbf{66.67\ \Omega}.$$

Consider two points *A* and *C* around the point of operation *B*. Then

$$r_{ac} = \frac{\Delta V}{\Delta I} = \frac{V_C - V_A}{I_C - I_A} = \frac{0.35 - 0.25}{(6-3) \times 10^{-3}} = \mathbf{33.33\ \Omega}.$$

Example 12. *The following table provides the set of values of V and I obtained for a given diode :*

	V	I
Forward biasing	2.0 V	60 mA
	2.4 V	80 mA
Reverse biasing	0 V	0 μA
	− 2 V	− 0.25 μA

Assuming the characteristics to be nearly linear, over this range, calculate the forward and reverse bias resistance of the given diode. [CBSE D 07C]

Solution. *For forward biasing :*

$$\Delta V = 2.4 - 2.0 = 0.4 \text{ V}; \quad \Delta I = 80 - 60 = 20 \text{ mA}$$

$$\therefore \quad r_{fb} = \frac{\Delta V}{\Delta I} = \frac{0.4 \text{ V}}{20 \times 10^{-3} \text{ A}} = \mathbf{20\ \Omega.}$$

For reverse biasing :

$$\Delta V = -2 - 0 = -2 \text{ V}$$

$$\Delta I = -0.25 - 0 = -0.25\ \mu\text{A}$$

$$\therefore \quad r_{rb} = \frac{-2 \text{ V}}{-0.25 \times 10^{-6} \text{ A}} = \mathbf{8 \times 10^6\ \Omega.}$$

Example 13. *The V-I characteristic of a silicon diode is given in Fig. 14.43. Calculate the diode resistance in : (a) forward bias at V = ± 2 V and V = + 1 V, and (b) reverse bias V = − 1 V and − 2 V.* [NCERT, CBSE F 04]

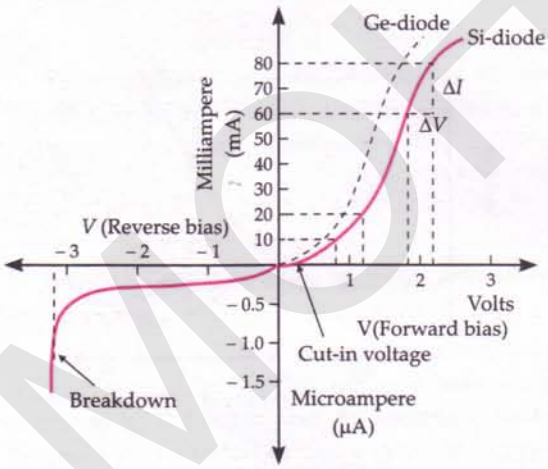


Fig. 14.43 Typical V-I characteristics of silicon and germanium diodes.

Solution. (*a*) The forward bias diode resistance is given by

$$r_{fb} = \frac{\Delta V}{\Delta I}$$

where ΔV and ΔI are the small changes in the voltage and current near the desired values.

$$r_{fb}\ (at + 2 \text{ V}) = \frac{(2.2 - 1.8) \text{ V}}{(80 - 60) \text{ mA}} = \frac{0.4 \text{ V}}{20 \times 10^{-3} \text{ A}} = \mathbf{20\ \Omega}$$

$$r_{fb}\ (at + 1 \text{ V}) = \frac{(1.2 - 0.8) \text{ V}}{(20 - 10) \text{ mA}} = \frac{0.4 \text{ V}}{10 \times 10^{-3} \text{ A}} = \mathbf{40\ \Omega.}$$

(*b*) In the reverse bias characteristic, the non-linearity in the *V-I* curve is small. The slopes of *V-I* curve at − 1 V and − 2 V are nearly equal.

$$r_{rb}\ (-2 \text{ V}) = \frac{-2 \text{ V}}{-0.25\ \mu\text{A}} = \frac{2 \text{ V}}{0.25 \times 10^{-6} \text{ A}}$$

$$= \mathbf{8 \times 10^6\ \Omega}$$

Also, $\quad r_{rb}\ (-1 \text{ V}) \approx \mathbf{8 \times 10^6\ \Omega.}$

Example 14. *A p-n junction diode when forward biased has a drop of 0.5 V which is assumed to be independent of current. The current in excess of 10 mA through the diode produces a large Joule heating which damages (burns) the diode. If we want to use a 1.5 V battery to forward bias the diode, what should be the value of resistor used in series with the diode so that the maximum current does not exceed 5 mA ?* [NCERT]

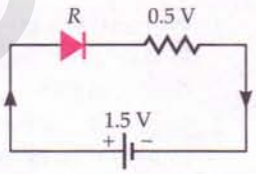


Fig. 14.44

Solution. Here $V_D = 0.5$ V, $V = 1.5$ V,

$$I = 5 \text{ mA} = 5 \times 10^{-3}, R = ?$$

The voltage equation for the diode circuit is

$$IR + V_D = V$$

or $\quad 5 \times 10^{-3} \text{A} \times R + 0.5 \text{ V} = 1.5 \text{ V}$

or $\quad R = \mathbf{200\ \Omega.}$

Example 15. *Draw the circuit to forward bias a diode. (The supply is 3 V and 100 mA battery). If the diode is made of silicon and knee voltage is 0.7 V, and a current of 20 mA passes through the diode, find the wattage of the resistor and the diode.*

Solution. The circuit for forward biased diode is shown in Fig. 14.45.

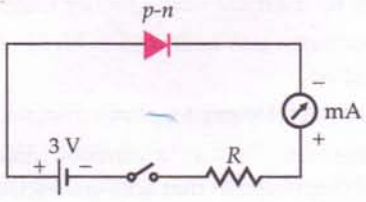


Fig. 14.45

Here emf of battery = 3 V

Knee voltage, $\quad V_k = 0.7$ V

$\therefore$ Voltage drop across $R = 3 - 0.7 = 2.3$ V

Current in the circuit, $I = 20$ mA $= 20 \times 10^{-3}$ A

Wattage of R = Voltage drop across $R \times$ Current

$= 2.3 \times 20 \times 10^{-3} =$ **0.046 W**

Wattage of diode

= Voltage drop across diode × current

$= 0.7 \times 20 \times 10^{-3} =$ **0.014 W.**

Example 16. *A battery of 2 V may be connected across the points A and B, as shown in Fig. 14.46. Find the current drawn from the battery if the positive terminal is connected to (i) the point A and (ii) the point B. Assume that the resistance of each diode is zero in forward bias and infinity in reverse bias.*

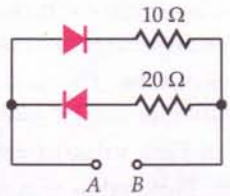


Fig. 14.46

Solution. (*a*) When positive terminal of the battery is connected to point *A*, diode D_1 gets forward biased and offers zero resistance and diode D_2 gets reverse biased and offers infinite resistance. The given circuit reduces to the equivalent circuit shown in Fig. 14.47.

$\therefore$ Current drawn from the battery,

$$I = \frac{2 \text{ V}}{10\ \Omega} = \textbf{0.2 A.}$$

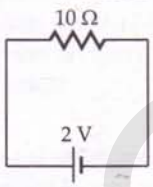


Fig. 14.47

Fig. 14.48

(*b*) When positive terminal of the battery is connected to point *B*, the diode D_1 gets reverse biased and offers infinite resistance and diode D_2 gets forward biased and offers zero resistance. The given circuit reduces to the equivalent circuit shown in Fig. 14.48.

$\therefore$ Current drawn from the battery,

$$I = \frac{2 \text{ V}}{20\ \Omega} = \textbf{0.1 A.}$$

Example 17. *Determine the currents through the resistances of the circuits shown in Fig. 14.49.*

Solution. (*i*) In Fig. 14.49(*a*), both the diodes D_1 and D_2 are forward biased and offer no resistance.

$\therefore$ Current in the circuit $= \dfrac{2.0 \text{ V}}{20\ \Omega} =$ **0.1 A**

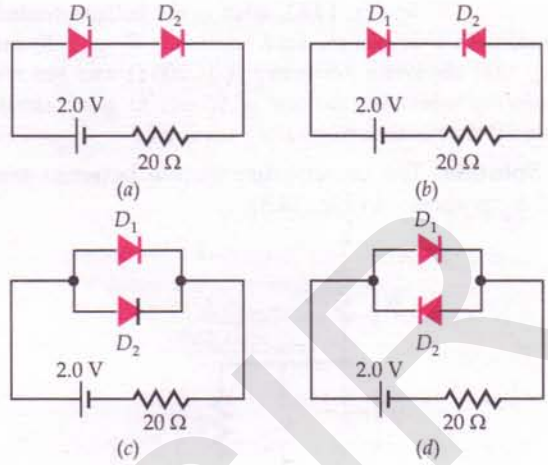


Fig. 14.49

(*ii*) In Fig. 14.49(*b*), diode D_2 being reverse biased offers infinite resistance, so current through the series circuit = **zero.**

(*iii*) In Fig. 14.49(*c*), D_1 and D_2 are forward biased and offer zero resistance.

$\therefore$ Current in the circuit $= \dfrac{2.0 \text{ V}}{20\ \Omega} =$ **0.1 A.**

(*iv*) In Fig. 14.49(*d*), no current flows through D_2 as it is reverse biased.

$\therefore$ Current in the remaining circuit $= \dfrac{2.0 \text{ V}}{20\ \Omega} =$ **0.1 A.**

Example 18. *A 10 V zener diode along with a series resistance is connected across a 40 V supply. Calculate the minimum value of the resistance required, if the maximum zener current is 50 mA.*

Solution. In Fig. 14.50, $V_i = 40$ V, $I_1 = 50$ mA

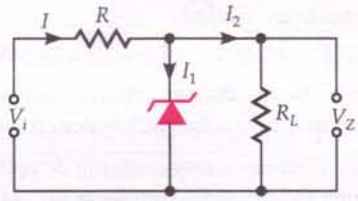


Fig. 14.50

$\therefore$ Maximum current,

$I = I_1 + I_2 = 50 + 0 = 50$ mA $= 50 \times 10^{-3}$ A

This is because maximum current flows through zener diode, so $I_2 = 0$.

V_z = Voltage drop across zener diode = 10 V

As I is maximum, so maximum value of R is

$$R = \frac{V_i - V_z}{I} = \frac{40 - 10}{50 \times 10^{-3}} = \textbf{600 Ω.}$$

Example 19. *In Fig. 14.51, what is the voltage needed to maintain 15 V across the load resistance R_L of 2 K, assuming that the series resistance R is 200 Ω and the zener requires a minimum current of 10 mA to work satisfactorily ? What is the zener rating required ?* [NCERT]

Solution. The current distribution between zener and R_L is shown in Fig. 14.51.

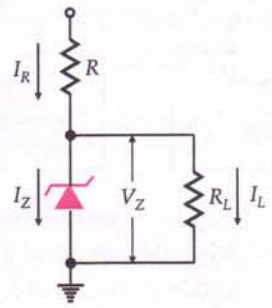


Fig. 14.51

Here load resistance, $R_L = 2\ k\Omega = 2 \times 10^3\ \Omega$

Voltage needed to maintain current across R_L,

$$V_L = 15\ V$$

Current through R_L,

$$I_L = \frac{V_L}{R_L} = \frac{15\ V}{2 \times 10^3\ \Omega}$$

$$= 7.5 \times 10^{-3}\ A = 7.5\ mA$$

Zener current, $I_Z = 10\ mA$

∴ Current through R,

$$I_R = I_Z + I_L = 10 + 7.5 = 17.5\ mA$$

Series resistance, $R = 200\ \Omega$

Voltage drop across R,

$$V_R = I_R \cdot R = 17.5 \times 10^{-3} \times 200 = 3.5\ V$$

∴ Input voltage needed,

$$V = V_R + V_L = 3.5 + 15 = \mathbf{18.5\ V.}$$

The zener diode chosen should have a current rating of **17.5 mA** and a breakdown voltage of **15 V**.

Example 20. *Find the average value of dc voltage that can be obtained from the half-wave rectifier of Fig. 14.52. Assume the diode to be ideal one.*

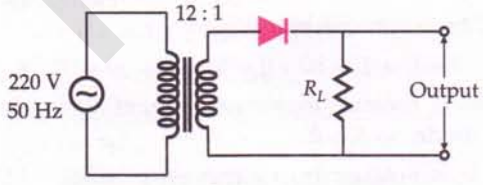


Fig. 14.52

Solution. The peak value of primary voltage is

$$V_0^P = \sqrt{2}\ V_{rms}^P = \sqrt{2} \times 220 = 311\ V$$

∴ The peak value of secondary voltage is

$$V_0^S = \frac{N_2}{N_1} \cdot V_0^P = \frac{1}{12} \times 311 = 25.9\ V$$

The d.c. voltage across the load is

$$V_{dc} = \frac{V_0^S}{\pi} = 0.637 \times 25.9 = \mathbf{8.24\ V.}$$

Example 21. *In a centre trap full wave rectifier, the load resistance $R_L = 1\ k\Omega$. Each diode has a forward bias dynamic resistance of 10 Ω. The voltage across half the secondary winding is 220 sin 314t. Find (i) the peak value of current (ii) the dc value of current and (iii) the rms value of current.*

Solution. The voltage across half the secondary winding is $V = 200 \sin 314\ t$

(*i*) Peak value of voltage, $V_0 = 220\ V$

∴ Peak value of current is

$$I_0 = \frac{V_0}{r_d + R_L} = \frac{220}{10 + 1000} = 0.2178\ A = \mathbf{217.8\ mA.}$$

(*ii*) d.c. value of current,

$$I_{dc} = \frac{2\ I_0}{\pi} = 2 \times 0.637 \times 217.8 = \mathbf{138.66\ mA.}$$

(*iii*) *rms* value of current is

$$I_{rms} = \frac{I_0}{\sqrt{2}} = 0.707 \times 217.8 = \mathbf{154\ mA.}$$

Problems For Practice

1. When the voltage drop across a *p-n* junction diode is increased from 0.70 V to 0.71 V, the change in the diode current is 10 mA. What is the dynamic resistance of the diode ? **[CBSE OD 94C]**

(Ans. 1 Ω)

2. The *V-I* characteristic of a silicon diode is as shown in Fig. 14.53. Calculate the resistance of the diode at (*i*) $I = 15$ mA and (*ii*) $V = -10$ V. **[NCERT ; CBSE F 15]**

[Ans. (*i*) 10 Ω (*ii*) 10 MΩ]]

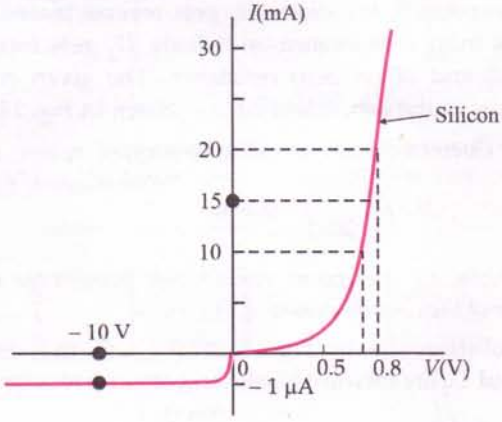


Fig. 14.53

3. A p-n junction is designed to withstand currents upto a maximum of 10 mA. A resistance of 200 Ω is connected in series with it. When forward biased, the diode has a potential drop of 0.5 V which is assumed to be independent of current. Find the maximum voltage of the battery to forward bias the diode. (Ans. 2.5 V)

4. The silicon diode shown in Fig. 14.54 is rated for a maximum current of 100 mA. Calculate the minimum value of resistor R. Assume the forward voltage drop across the diode to be 0.7 V.
(Ans. 93 Ω, a safer value of 100 Ω can be taken)

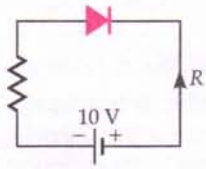


Fig. 14.54

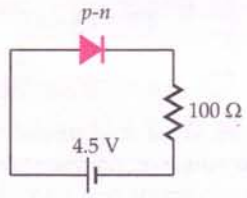


Fig. 14.55

5. Figure 14.55 shows a diode connected to an external resistance and a battery. Assuming that the barrier developed in the diode is 0.5 V, obtain the value of current in the circuit in milliampere. (Ans. 40 mA)

6. Find the current through the circuit and the potential difference across the diode shown in Fig. 14.56. The drift current for the diode is 20 μA.
(Ans. 20 μA, ≃ 4.0 V)

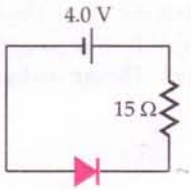


Fig. 14.56

Fig. 14.57

7. Find the equivalent resistance of the circuit shown in Fig. 14.57 between the points A and B.
(Ans. 10 Ω if $V_A > V_B$ and 20 Ω if $V_A < V_B$)

8. Assuming that the resistances of the meters are negligible, what will be the readings of the ammeters A_1 and A_2 in the circuit shown in Fig. 14.58 ?
(Ans. zero in A_1, 0.2 A in A_2)

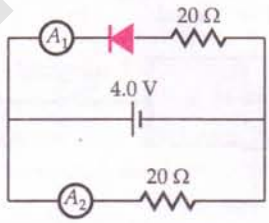


Fig. 14.58

9. A potential barrier of 0.60 V exists across a p-n junction. (*i*) If the depletion region is 6.0×10^{-7} m thick, what is the intensity of the electric field in this region ? (*ii*) If an electron with speed $5.0 \times 10^5 \text{ms}^{-1}$ approaches the p-n junction from the n-side, with what speed will it enter the p-side ?
[Ans. (*i*) $1.0 \times 10^8 \text{Vm}^{-1}$ (*ii*) $2.0 \times 10^5 \text{ms}^{-1}$]

10. A sinusoidal voltage of rms value 220 V is applied to a diode and a resistor R in the circuit shown in Fig. 14.59, so that half wave rectification occurs. If the diode is ideal, what is the rms voltage across R?
(Ans. $110\sqrt{2}$ V)

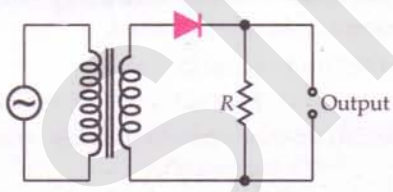


Fig. 14.59

11. The applied input a.c. to a half wave rectifier is 100 W. The d.c. output is 40 W. (*i*) What is the rectification efficiency ? (*ii*) What is the power efficiency ? [Ans. (*i*) 40% (*ii*) 80%]

12. A crystal diode having internal resistance 200 Ω is used as a half rectifier. If the applied voltage is $V = 50 \sin \omega t$ volt and load resistance is 800 Ω, find (*i*) maximum output current (*ii*) d.c. output current (*iii*) d.c. output power and (*iv*) d.c. output voltage.
[Ans. (*i*) 61 mA (*ii*) 19.4 mA
(*iii*) 0.301 W (*iv*) 15.52 V]

13. In a photodiode, the conductivity increases when the material is exposed to light. It is found that conductivity changes only if the wavelength is less than 600 nm. What is the band gap ? (Ans. 1.995 eV)

HINTS

1. $r_d = \dfrac{\Delta V}{\Delta I} = \dfrac{(0.71 - 0.70)\text{ V}}{10\text{ mA}} = \dfrac{0.01\text{ V}}{10 \times 10^{-3}\text{ A}} = \mathbf{1\,\Omega.}$

2. Considering the diode characteristics as a straight line between $I = 10\text{mA}$ to $I = 20\text{mA}$, we can calculate the resistance using ohm's law.

(*i*) From the curve, at $I = 20\text{mA}$, $V = 0.8$ V and at $I = 10$ mA, $V = 0.7$ V.

$$\therefore\ r_{fb} = \frac{\Delta V}{\Delta I} = \frac{(0.8 - 0.7)\text{V}}{(20 - 10)\text{mA}} = \frac{0.1\text{V}}{10 \times 10^{-3}\text{A}} = \mathbf{10\,\Omega.}$$

(*ii*) From the curve, at $V = -10$ V, $I = -1\,\mu\text{A}$

$$\therefore\ r_{rb} = \frac{V}{I} = \frac{10\text{ V}}{1\,\mu\text{A}} = \frac{10\text{ V}}{1\,\mu\text{A}} = \frac{10\text{ V}}{10^{-6}\text{ A}} = 10^7\,\Omega = \mathbf{10\ M\Omega.}$$

3. If V is the maximum forward biased voltage, then
$V - 0.5 = 10\text{ mA} \times 200\,\Omega = 2\text{ V}$
or $V = 2 + 0.5 = \mathbf{2.5\text{ V}}$.

4. The current through the diode should not exceed 100 mA.
$\therefore \quad IR = V - 0.7$
$100 \times 10^{-3} R = 10 - 0.7 = 9.3$
or $R = \dfrac{9.3}{0.1} = \mathbf{93\,\Omega}$.

5. $I = \dfrac{V_{net}}{R} = \dfrac{4.5 - 0.5}{100} = 4 \times 10^{-2}\text{ A} = \mathbf{40\text{ mA}}$

6. As the diode is reverse biased, only drift current exists in circuit which is 20 μA.
Potential drop across 15 Ω resistor
$= 15\,\Omega \times 20\,\mu\text{A} = 300\,\mu\text{V} = 0.0003\text{ V}$
Potential difference across the diode = 4.0 – 0.0003
$= 3.9997 \simeq \mathbf{4.0\text{ V}}$.

7. When $V_A > V_B$, the diode gets forward biased and offers no resistance.
$\therefore \quad R = \dfrac{20 \times 20}{20 + 20} = \mathbf{10\,\Omega}$
When $V_A < V_B$, the diode gets reverse biased and offers infinite resistance. No current flows through the upper branch.
$\therefore \quad R = \mathbf{20\,\Omega}$.

8. In the given circuit, the diode is reverse biased. No current flows through the upper resistance.
$\therefore$ Reading of ammeter $A_1 = 0$.
Reading of ammeter $A_2 = \dfrac{4\text{ V}}{20\,\Omega} = \mathbf{0.2\text{ A}}$.

9. (*i*) $E = \dfrac{V}{d} = \dfrac{0.60}{6.0 \times 10^{-7}} = \mathbf{1.0 \times 10^8\ Vm^{-1}}$.

(*ii*) $\dfrac{1}{2} m v_1^2 = eV + \dfrac{1}{2} m v_2^2$
or $\dfrac{1}{2} \times 9.1 \times 10^{-31} \times (5.0 \times 10^5)^2$
$= 1.6 \times 10^{-19} \times 0.6 + \dfrac{1}{2} \times 9.1 \times 10^{-31} \times v_2^2$
On solving,
$v_2 = 1.975 \times 10^5\ \text{ms}^{-1}$
$\simeq \mathbf{2.0 \times 10^5\ ms^{-1}}$.

10. The output rms voltage obtained from a half wave rectifier is
$V_{rms} = \dfrac{V_0}{2} = \dfrac{220\sqrt{2}}{2} = \mathbf{110\sqrt{2}\text{ V}}$.

11. (*i*) Rectification efficiency
$= \dfrac{\text{d.c. output power}}{\text{a.c. input power}} = \dfrac{40}{100} = \mathbf{40\%}$

(*ii*) Power efficiency
$= \dfrac{\text{d.c. output power}}{\text{a.c. input power for half cycle}} = \dfrac{40}{50} = \mathbf{80\%}$.

12. (*i*) $I_0 = \dfrac{V_0}{r_d + R_L}$ (*ii*) $I_{dc} = \dfrac{I_0}{\pi}$
(*iii*) d.c. output power $= I_{dc}^2 \cdot R_L$
(*iv*) d.c. output voltage $= I_{dc} \cdot R_L$

13. $E_g = \dfrac{hc}{\lambda} = \dfrac{6.6 \times 10^{-34} \times 3 \times 10^8}{620 \times 10^{-9}}\text{ J}$
$= \dfrac{6.6 \times 3 \times 10^{-17}}{620 \times 1.6 \times 10^{-19}}\text{ eV} = \mathbf{1.995\text{ eV}}$.

14.32 JUNCTION TRANSISTOR

36. *What is a transistor ? Mention its two types. Give their symbolic representations. Describe the construction of a transistor and state the function of its each part.*

Transistor. *A junction transistor is a three terminal solid state device obtained by growing either a narrow section of p-type crystal between two relatively thicker sections of n-type crystals or a narrow section of n-type crystal between two thicker sections of p-type crystals.*

Transistor was first invented by *J. Bardeen* and *W.H. Brattain* of Bell Telephone Laboratories, U.S.A.

Transistors are of *two* types :

1. ***n-p-n transistor.*** *It consists of a thin section of p-type semiconductor sandwitched between two thicker sections of n-type semiconductors.* Fig. 14.60 shows the *n-p-n* transistor and its circuit symbol. The arrowhead in the symbol points *outwards*.

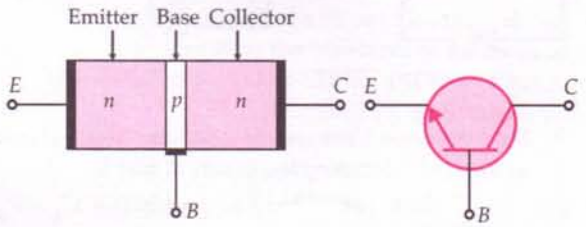


Fig. 14.60 *n–p-n* transistor and its circuit symbol.

2. ***p-n-p transistor.*** *It consists of a thin section of n-type semiconductor sandwitched between two thicker*

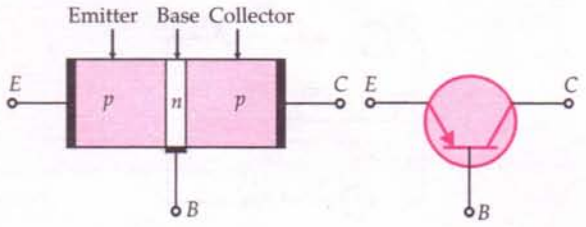


Fig. 14.61 *p–n-p* transistor and its circuit symbol.

sections of p-type semiconductors. Fig. 14.61 shows the *p-n-p* transistor and its circuit symbol. The arrowhead in the symbol points *inwards.*

In both types of transistors, the arrowhead on the emitter points in the direction of conventional current.

Construction. Each type of transistor has three main parts :

1. ***Emitter (E).*** It is a section on one side of the transistor. It is of *moderate size* and *heavily doped* semiconductor. It is normally *forward biased* w.r.t. any other part of the transistor. It supplies a large number of *majority charge carriers* for the flow of current through the transistor.

2. ***Base (B).*** It is the middle section. It is *very thin* and lightly doped. It controls the flow of majority charge carriers from emitter to collector.

3. ***Collector (C).*** It is section on the other side of the transistor. It is *moderately doped* and larger in size as compared to the emitter. It is normally *reverse* biased w.r.t. any other part of the transistor. It collects the majority charge carriers for the circuit operation.

Figure 14.62 shows the relative sizes of the three regions of the *n-p-n* transistor and the biasing of base-emitter and base-collector junctions. The forward bias voltage V_{EB} is small (0.5 to 1 V) while the reverse bias voltage V_{CB} is high (5 to 15 V).

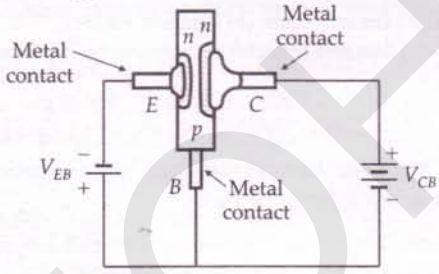


Fig. 14.62 Relative sizes of the three regions of the *n-p-n* transistor and the biasing.

14.33 ACTION OF *n-p-n* TRANSISTOR

37. *With a proper circuit diagram, show the biasing of n-p-n transistor. Explain the transistor action.*

Action of *n-p-n* transistor. The *n*-type emitter of *n-p-n* transistor is forward biased by connecting it to the –ve terminal of battery V_{EB} and the *n*-type collector is reverse biased by connecting it to the +ve terminal of battery V_{CB}, as shown in Fig. 14.63.

The forward bias of the emitter-base circuit repels the electrons of emitter towards the base, setting up emitter current I_E. As the base is very thin and lightly doped, a very few electrons (< 5%) from the emitter combine with the holes of base, giving rise to base

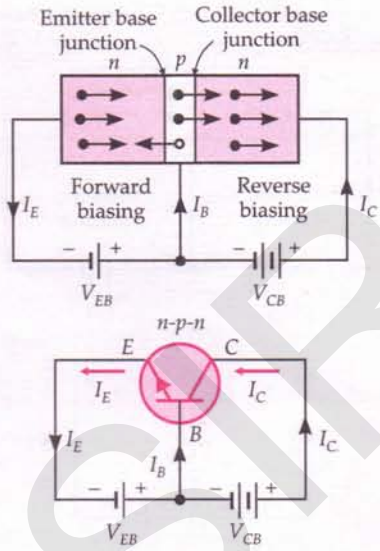


Fig. 14.63 Action of *n-p-n* transistor and its biasing.

current I_B and the remaining electrons (>95%) are pulled by the collector which is at high positive potential. The electrons are finally collected by the +ve terminal of battery V_{CB}, giving rise to collector current I_C.

As soon as an electron from the emitter combines with a hole in the base region, an electron leaves the negative terminal of the battery V_{EB} and at the same time the positive terminal of battery V_{EB} receives an electron from the base. This sets a base current I_B. Similarly, corresponding to each electron that goes from collector to positive terminal of V_{CB}, an electron enters the emitter from negative terminal of V_{EB}. Hence

Emitter current = Base current + Collector current

or $$I_E = I_B + I_C \qquad [I_B << I_C]$$

Here I_B is a small fraction of I_C depending on the shape of transistor, thickness of base, doping levels, bias voltages, etc.

14.34 ACTION OF *p-n-p* TRANSISTOR

38. *With a proper circuit diagram, show the biasing of p-n-p transistor. Explain the transistor action.*

Action of *p-n-p* transistor. The *p*-type emitter of *p-n-p* transistor is forward biased by connecting it to the +ve terminal of battery V_{EB} and the *p*-type collector is reverse biased by connecting it to the –ve terminal of battery V_{CB}, as shown in Fig. 14.64.

The forward bias of the emitter-base circuit repels the holes of emitter towards the base and electrons of base towards the emitter. As the base is very thin and lightly doped, most of the holes (>95%) entering it pass on to collector while a very few of them (<5%) recombine with the electrons of the base region.

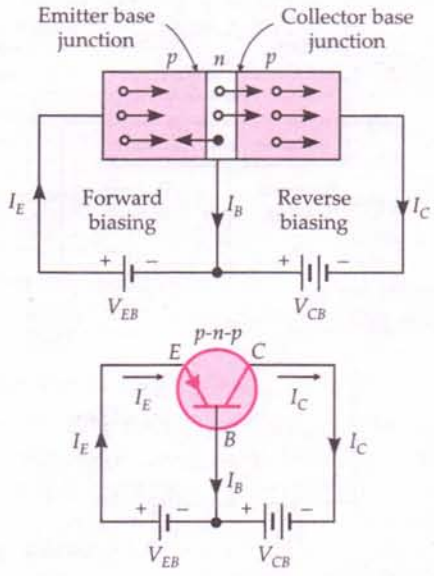


Fig. 14.64 Action of *p-n-p* transistor and its biasing.

As soon as a hole combines with an electron, an electron from the negative terminal of the battery V_{EB} enters the base. This sets up a small base current I_B. Each hole entering the collector region combines with an electron from the negative terminal of the battery V_{CB} and gets neutralised. This creates collector current I_C. Both the base current I_B and collector current I_C combine to form emitter current I_E.

$$\therefore \quad I_E = I_B + I_C$$

Thus inside the *p-n-p* transistor, the current conduction is due to holes while electrons are the charge carriers in the external circuit.

14.35 THREE CONFIGURATIONS OF A TRANSISTOR

39. *Draw the three types of circuit arrangements in which an n-p-n transistor can be used.*

Three configurations of a transistor. A transistor is a three element device. One terminal has to be always common to the input and the output circuits. This terminal is connected to the ground and serves as a reference point for the entire circuit. So a transistor can be used in one of the following *three* configurations :

1. Common-base (CB) circuit.
2. Common-emitter (CE) circuit.
3. Common-collector (CC) circuit.

Fig. 14.65 shows the three types of circuit arrangements for an *n-p-n* transistor. In each case, the emitter-base junction is forward biased while the collector-base junction is reverse biased.

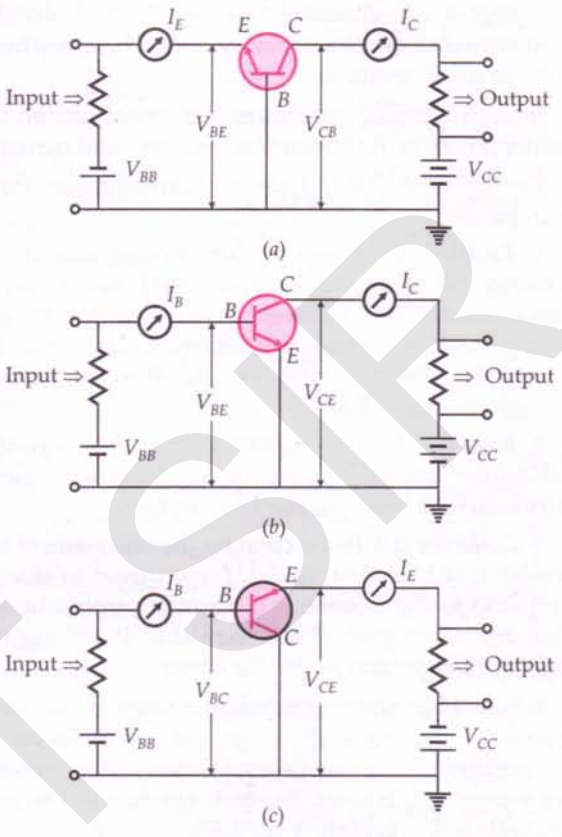


Fig. 14.65 (*a*) Common-base (*b*) Common-emitter, (*c*) Common-collector connections for *n-p-n* transistor.

14.36 CURRENT GAINS IN A TRANSISTOR

40. *Define the two current gains of a transistor and deduce a relation between them.*

Current gains in a transistor. Usually *two* types of current gains are defined for a transistor :

1. Common base current amplification factor or a.c. current gain α. *It is defined as the ratio of the small change in the collector current to the small change in the emitter current when the collector-base voltage is kept constant.* Thus

$$\alpha = \left[\frac{\Delta I_C}{\Delta I_E}\right]_{V_{CB}=\text{constant}}$$

2. Common emitter current amplification factor or a.c. current gain β. *It is defined as the ratio of the small change in the collector current to the small change in the base current when the collector-emitter voltage is kept constant.* Thus

$$\beta = \left[\frac{\Delta I_C}{\Delta I_B}\right]_{V_{CE}=\text{constant}}$$

Relation between α and β. For both *n-p-n* and *p-n-p* transistors, we have

$$I_E = I_B + I_C$$

For small changes, we can write

$$\Delta I_E = \Delta I_B + \Delta I_C$$

Dividing both sides by ΔI_C,

$$\frac{\Delta I_E}{\Delta I_C} = \frac{\Delta I_B}{\Delta I_C} + 1$$

or $$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \qquad \left[\because \frac{\Delta I_C}{\Delta I_E} = \alpha \; ; \; \frac{\Delta I_C}{\Delta I_B} = \beta\right]$$

or $$\alpha = \frac{\beta}{1+\beta}$$

and $$\beta = \frac{\alpha}{1-\alpha}$$

As the value of I_B is about 1 – 5% of I_E or I_C is 95 – 99% of I_E, α is about 0.95 to 0.99 and β is about 20 to 100. The *CE* configuration is frequently used as it gives high current gain as well as voltage gain.

NOTE **1.** α and β are independent of current if the emitter-base junction is forward biased and the collector-base junction is reverse biased.

2. The above definitions of α and β do not hold when both the junctions of a transistor are forward biased or reverse biased.

14.37 COMMON EMITTER CHARACTERISTICS

41. *Draw a circuit diagram for an n-p-n transistor in common emitter configuration to study its (i) input, (ii) output and (iii) transfer characteristics. Draw approximate shape of these curves and give their important features. How will you use these characteristics to obtain (i) input resistance, (ii) output resistance and (iii) current amplification factor ?*

Common emitter characteristics. *The common-emitter characteristics are the graphs drawn between appropriate voltages and currents for a transistor when its emitter is taken as the common terminal and grounded (zero potential), base is the input terminal and collector is the output terminal.*

Figure 14.66 shows the circuit diagram for studying the common emitter characteristics of an *n-p-n* transistor. The emitter-base junction is forward biased by means of battery V_{BB} through rheostat Rh_1. The emitter-collector circuit is reverse biased by means of battery V_{CC} through rheostat Rh_2. The base-emitter voltage V_{BE} and the collector-emitter voltage V_{CE} are measured by high resistance voltmeters. The base current I_B is measured by a microammeter and the collector current I_C by a milliammeter. Three types of characteristic curves are studied.

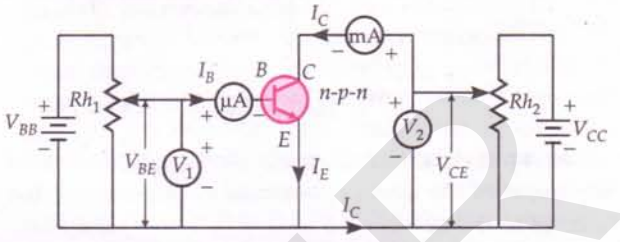


Fig. 14.66 Circuit for studying the common emitter characteristics of an *n–p-n* transistor.

1. Input characteristic. *A graph showing the variation of base current I_B with base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE} is called the input characteristic of the transistor.* Two such curves for two different collector-emitter voltages have been plotted in Fig. 14.67.

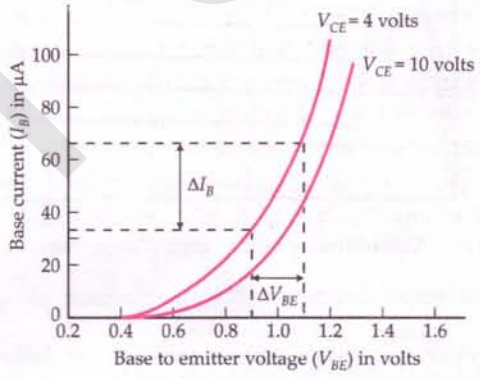


Fig. 14.67 Input characteristics of *CE n-p-n* transistor.

A study of these curves reveals the following facts :

(*i*) As long as V_{BE} is less than the barrier voltage, the base current I_B is small as in the case of forward biased diode.

(*ii*) When the base-emitter voltage V_{BE} exceeds the barrier voltage, the base current I_B increases sharply with a small increase in V_{BE} as in the case of a forward biased diode.

(*iii*) The value of I_B is much smaller than that in a normal diode, more than 95% majority emitter carriers (electrons in *n-p-n* and holes in *p-n-p* transistor) go to the collector to constitute the collector current I_C.

Since the increase in V_{CE} appears as the increase in V_{CB}, its effect on I_B is negligible. As a result, input characteristics for various values of V_{CE} give almost identical curves. Hence, *it is enough to determine only one input characteristic.*

The input resistance r_i *of the transistor in CE configuration is defined as the ratio of the small change in base-emitter voltage to the corresponding small change in the base current, when the collector-emitter voltage is kept fixed.* Thus

$$r_i = \left[\frac{\Delta V_{BE}}{\Delta I_B}\right]_{V_{CE} = \text{constant}}$$

As input characteristic is non-linear, so r_i varies. At any point of the curve, r_i is equal to the slope of the tangent to the curve.

2. Output characteristic. *A graph showing the variation of collector current I_C with collector-emitter voltage V_{CE} at constant base-current I_B is called the output characteristic of the transistor.* Fig. 14.68 shows such curves for different values of I_B.

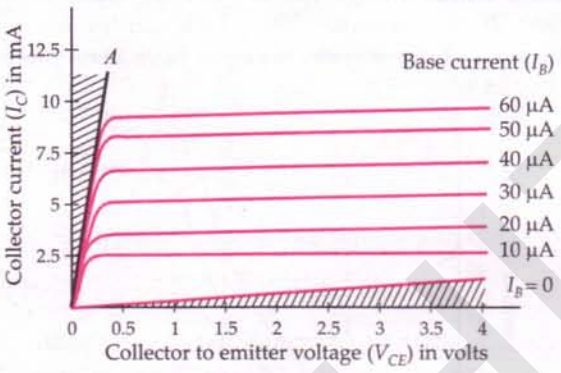


Fig. 14.68 Output characteristic of *CE n-p-n* transistor.

A study of these curves reveals the following features :

(*i*) When the voltage V_{CE} increases from 0 to about 0.5 V, the collector current I_C increases rapidly. The value of V_{CE} upto which I_C increases rapidly is called *knee voltage.*

(*ii*) Once the voltage V_{CE} exceeds the voltage V_{BE} (so that the collector-base junction is reverse biased), the output current I_C varies *very slowly* but *linearly* with V_{CE} for a given base current I_B, *i.e.,* beyond the knee voltage the output resistance of the transistor is high.

(*iii*) Larger the value of I_B, larger is the value of I_C for a given V_{CE}.

Three regions of the output characteristic :

(*a*) The shaded region towards the left of line *OA* is called ***saturation region*** and the line *OA* is called ***saturation line***. Here $V_{CE} < V_{BE}$. Both the junctions are forward biased. Here I_C does not depend on the input current I_B.

(*b*) The shaded region lying below the curve for $I_B = 0$ is called *cut-off region.* In this region, both the junctions are reverse biased. Here $I_C = 0$. In the shaded regions, the transistor works as ***switch***, *it turns over rapidly from OFF state for which $I_C = 0$ (**cut-off**) to the ON state for which I_C is maximum (saturation state).*

(*c*) The non-shaded central region of the output characteristic is called ***active region***. In this region, the emitter-base junction is forward biased and the collector-base junction is reverse biased. A transistor works as an ***audio amplifier*** in this region.

The **output resistance** r_0 *of a transistor in CE configuration is defined as the ratio of the small change in the collector-emitter voltage to the corresponding change in the collector current when the base current is kept constant.* Thus

$$r_0 = \left[\frac{\Delta V_{CE}}{\Delta I_C}\right]_{I_B = \text{constant}}$$

3. Transfer characteristic. *It is a graph showing the variation of collector current I_C with base current I_B at constant collector-emitter voltage V_{CE}.* As shown in Fig. 14.69, the transfer characteristic of a transistor is almost a straight line.

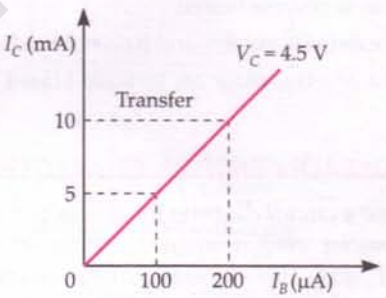


Fig. 14.69 Transfer characteristic of *CE n-p-n* transistor.

Current amplification factor (β). *It is defined as the ratio of the change in collector current to the small change in base current at constant collector-emitter voltage (V_{CE}) when the transistor is in the active state.*

$$\beta_{ac} = \left[\frac{\Delta I_C}{\Delta I_B}\right]_{V_{CE} = \text{constant}}$$

This is also known as small ***signal current gain*** and its value is very large. The direct ratio of I_C and I_B gives the ***dc current gain*** (β_{dc}) of the transistor. Hence,

$$\beta_{dc} = \frac{I_C}{I_B}$$

Since I_C increases with I_B almost linearly and $I_C = 0$ when $I_B = 0$, *the values of both β_{ac} and β_{dc} are nearly equal.*

14.38 TRANSISTOR AS A SWITCH

42. *Explain the use of a transistor as a switch.*

Transistor as a switch. Digital devices like computers perform millions of switching operations every day. Transistors can be used as such swift switches in computer circuits.

Transistors have many advantages over other electrically operated switches such as relays and reed switches.

1. Transistors are small, cheap and reliable.
2. They have no moving parts.
3. They have long life in well-designed circuits.
4. They can switch on and off millions of times a second.

Three states of a transistor. To understand the operation of a transistor as a switch, we first study the three states or conditions in which a transistor can work. Fig. 14.70(*a*) shows the circuit diagram of a base-biased *n-p-n* transistor in CE configuration. Here R_B is a resistor in the input circuit and R_C in the output circuit.

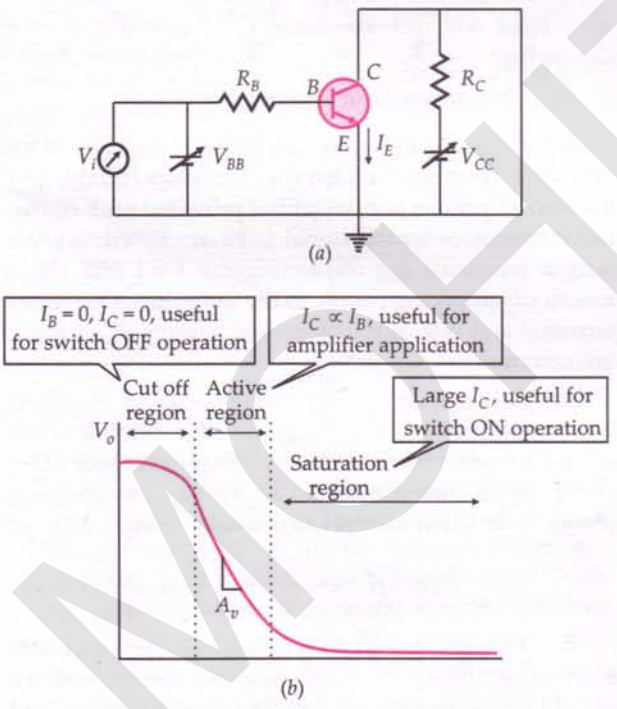


Fig. 14.70 (*a*) A base biased *n-p-n* transistor in *CE* configuration. (*b*) Transfer characteristic of base-biased transistor.

Applying Krichhoff's rule to the input and output circuits separately, we get

$$V_{BB} = I_B R_B + V_{BE}$$

and $$V_{CC} = I_C R_C + V_{CE}$$

or $$V_{CE} = V_{CC} - I_C R_C$$

The voltage V_{BB} can be regarded as the dc input voltage V_i and V_{CE} as the dc output voltage V_0. So we can write

$$V_i = I_B R_B + V_{BE}$$

and $$V_o = V_{CC} - I_C R_C \quad ...(1)$$

Figure 14.70(*b*) shows typical output voltage (V_0) – input voltage (V_i) characteristic, called the ***transfer characteristic*** of the base biased transistor. It has three well-defined regions as follows :

1. ***Cut off region.*** When V_i increases from zero to a low value (less than 0.6 V in case of a Si transistor), the forward bias of the emitter-base junction is insufficient to start a forward current. That is, $I_B = 0$ and hence $I_C = 0$. The transistor is said to be in the *cut off region*. From equation (1), the output voltage $V_o = V_{CC}$.

2. ***Active region.*** When V_i increases slightly above 0.6 V, a current I_C flows in the output circuit and the transistor is said to be in the active state. From equation (1), as the term $I_C R_C$ increases, the output voltage V_o decreases. Now as V_i increases, I_C increases almost linearly and so V_o decreases linearly till its value becomes less than 1.0 V.

3. ***Saturation region.*** When V_i is high *i.e.*, the emitter-base junction is heavily forward biased, a large collector current I_C flows which produces such a large potential drop across load resistance R_C that the emitter-collector junction also gets forward biased. The output voltage V_o decreases to almost zero. The transistor is said to be in the saturation state because it cannot pass any more collector current I_C.

Obviously, the transitions from cut off state to active state and from active state to saturation state are not sharply defined because these regions of the transfer characteristic are non-linear.

Switching action of a transistor. A transistor can be used as a switch if it is operated in its cut off and saturation states only. A switch circuit is designed in such a manner that the transistor does not remain in the active state. As long as the input voltage is low and unable to forward-bias the transistor, the output voltage V_o (at V_{CC}) is high. If V_i is high enough to drive the transistor into saturation, then V_o is low, nearly zero. When the transistor is not conducting, it is said to be ***switched off*** and when it is driven into saturation, it is said to be ***switched on***. So if we define low (0) and high (1) states as below and above certain voltage levels corresponding to cut off and saturation of the transistor, then a low input switches the transistor off and a high input switches it on. Alternatively, we can say that a low input to the transistor gives a high output and high input gives a low output.

14.39 CONCEPT OF AN AMPLIFIER

43. *What do you mean by the amplifying action of a transistor ? Why is a transistor so called ? Why is the base region of a transistor made very thin and lightly doped ? Define transconductance of a transistor.*

Amplifying action of a transistor. As the base-emitter junction of a transistor is forward biased, the depletion layer about this junction is much smaller than the depletion layer around the base-collector junction which is reverse biased. Thus the resistance R_{EB} of the emitter-base junction is much smaller than the resistance R_{BC} of the collector-base junction.

$\therefore$ Power dissipation in the emitter-base circuit,

$$P_{EB} = I_E^2 R_{EB}.$$

Power dissipation in the base-collector circuit,

$$P_{BC} = I_C^2 R_{BC}$$

Now $I_E \simeq I_C$ and $R_{BC} >> R_{EB}$,

$\therefore$ $P_{BC} >> P_{EB}$

i.e., the power dissipated in the base-collector circuit is much higher than the power dissipated in the emitter-base circuit or *output power is much greater than the input power. This is the amplifying action of a transistor.*

Why is a transistor so called ? The collector current I_C is almost equal to the emitter current I_E. But the resistance offered by the emitter-base junction to the flow of current is small as it is forward biased. The resistance offered by the base-collector junction to the flow of current is large because this junction is reverse biased. *The current is thus transferred from a low resistance circuit to a high resistance circuit. Hence the name transistor, which is combination of the words* ***transfer*** *and* ***resistor****.*

The base region of a transistor is very thin and lightly doped. A thin and lightly doped base region contains a smaller number of majority charge carriers. This reduces the rate of recombination of electrons and holes at the emitter-base junction. Most (95 – 99%) of the majority charge carriers, diffusing from emitter to base, reach the collector. Thus the base current is small and the collector is almost equal to the emitter current. This results in the large voltage gain and power gain of the transistor.

In a voltage amplifier, the input signal to be amplified is superposed on a steady voltage V_{EB} applied across the emitter-base junction. For a high voltage gain (the ratio of output voltage to the input voltage), the change in the collector current (ΔI_c) should be as large as possible for a given change in the emitter-base voltage (ΔV_{EB}). So we can define a figure of merit for a transistor as follows :

Transconductance. *It is defined as the ratio of the small change in the collector current to the small change in the emitter-base voltage.* It is denoted by g_m. Thus

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}}$$

The transconductance is also called ***transfer conductance*** and has the same units of conductance (siemen or mho). The transconductance depends on the geometry, doping levels and biasing of the transistor.

44. *What is an amplifier ? Define its voltage gain.*

Concept of an amplifier. *An* **amplifier** *is a circuit (consisting of at least one transistor) which is used for increasing the voltage, current or power of alternating form.*

To amplify means to increase the size or to magnify an input signal. The output signal of an amplifier is an enlarged version of the input signal.

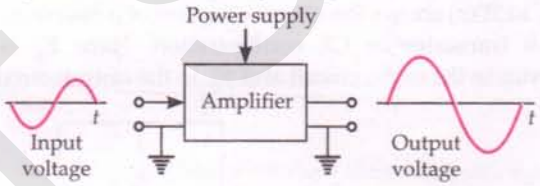


Fig. 14.71 The concept of an amplifier.

Figure 14.71 illustrates the general concept of an amplifier. Here the *black box* (*i.e.,* the unspecified object marked amplifier) is an amplifier provided with (*i*) two input terminals for the signal to be amplified, (*ii*) two output terminals for connecting the load and (*iii*) a means of supplying power to the amplifier. One input terminal and one output terminal (shown as earthed) are common.

AC voltage gain A_v. The usefulness of an amplifier is expressed in terms of the gain of the amplifier. The *a.c. voltage gain of an amplifier is defined as the ratio of the change in the output voltage* (ΔV_0) *to the corresponding change in the input voltage* (ΔV_i). Thus

$$A_v = \frac{\Delta V_0}{\Delta V_i}$$

The voltage gain of an amplifier is always greater than unity. It may be noted that only the *a.c.* and not the *d.c.* components of the input and the output voltages are used to calculate the voltage gain.

14.40 TRANSISTOR AS A COMMON BASE AMPLIFIER*

45. *With the help of a labelled circuit diagram, describe the use of n-p-n transistor as a common base amplifier. Discuss the phase relationship between input and output voltages. Write expressions for various current gains of a common base amplifier.*

n-p-n transistor as a common-base amplifier. Figure 14.72 shows the use of *n-p-n* transistor as a common base amplifier. The base is common to both input and output circuits. The emitter is forward biased by battery V_{EE} and the collector is reverse biased by battery V_{CC}.

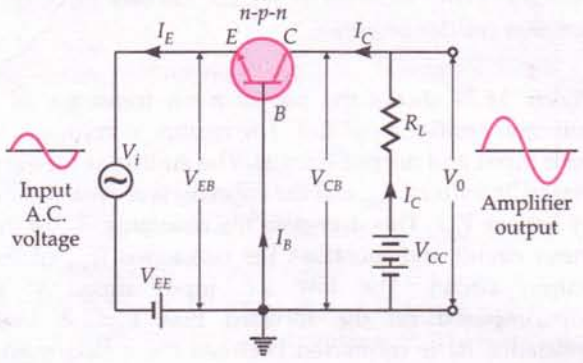


Fig. 14.72 *n-p-n* transistor as a common base amplifier.

This decreases the resistance R_{in} of the input circuit and increases the resistance R_{out} of the output circuit. So $R_{out} > R_{in}$. The low input a.c. signal is superimposed on the forward bias V_{EB}. A load resistance R_L is connected between the collector and d.c. supply. The amplified output is obtained between collector and ground. When no a.c. signal is fed to the input circuit, we have

$$I_E = I_B + I_C$$

When a current I_C flows in the circuit, a voltage drop $I_C R_L$ occurs across the load R_L. The output voltage will be

$$V_0 = V_{CB} = V_{CC} - I_C R_L$$

When the input signal V_i is applied in emitter-base circuit, it changes the emitter-base voltage and the emitter current I_E. This, in turn, changes the collector current I_C and hence the output voltage V_0 in accordance with the above relation. This variation in the collector-base voltage appears as amplified output.

Phase relationship between input and output signals. When a.c. signal is fed to the input circuit, its positive half cycle decreases the forward bias. This decreases the emitter current and the collector current. The potential drop $I_C R_L$ across load resistance decreases. The output signal V_0 becomes more positive. So as the input signal goes through its positive half cycle, the output signal also goes through a positive half cycle. Similarly, as the input signal goes through its negative half cycle, the output signal also goes through its negative half cycle. Hence in a common base amplifier, the input and output voltages are in same phase.

Current, voltage and power gains of a common base amplifier :

a.c. current gain. *It is defined as the ratio of the small change in the collector current (ΔI_C) to the small change in the emitter current (ΔI_E), when the collector-base voltage is kept constant.*

$$\alpha_{ac} \quad \text{or} \quad A_i = \left[\frac{\Delta I_C}{\Delta I_E}\right]_{V_{CB}=\text{constant}}$$

d.c. current gain. It is defined as the ratio of the collector current to the emitter current, when the collector-base voltage is constant.

$$\alpha_{dc} = \left[\frac{I_C}{I_E}\right]_{V_{CB}=\text{constant}}$$

a.c. voltage gain. It is *defined as the ratio of the small change in output voltage (ΔV_{CB}) to the small change in input voltage ΔV_{EB}.* It is given by

$$A_v = \frac{\Delta V_{CB}}{\Delta V_{EB}}$$

But $\Delta V_{CB} = R_0 \cdot \Delta I_C$

and $\Delta V_{EB} = R_i \, \Delta I_E$

where R_i is the resistance of input circuit and R_0 is the resistance of output circuit (including R_L).

$$\therefore \quad A_v = \frac{\Delta I_C}{\Delta I_E} \cdot \frac{R_o}{R_i} = \alpha_{ac} \cdot \frac{R_o}{R_i}$$

or $A_v = A_i \cdot A_r$

or Voltage gain = Current gain × Resistance gain.

a.c. power gain. *It is defined as the ratio of the small change in output power to the small change in input power.*

$$\text{a.c. power gain} = \frac{\text{Change in output power}}{\text{Change in input power}}$$

$$= \frac{(\Delta I_C)^2 \, R_0}{(\Delta I_E)^2 \, R_i}$$

or $$A_p = \alpha_{ac}^2 \frac{R_0}{R_i} = \alpha_{ac}^2 \times \text{resistance gain.}$$

46. *Explain with the help of a labelled circuit diagram, the use of p-n-p transistor as a common base amplifier. Discuss the phase relation between input and output voltages.*

p-n-p transistor as a common base amplifier. Figure 14.73 shows the use of *p-n-p* transistor as a common base amplifier. The emitter is common to both input and output circuits. The emitter is forward biased by battery V_{EE} and the collector is reverse

biased by battery V_{CC}. This decreases the resistance R_{in} of the input circuit and increases the resistance R_{out} of the output circuit. So $R_{out} > R_{in}$.

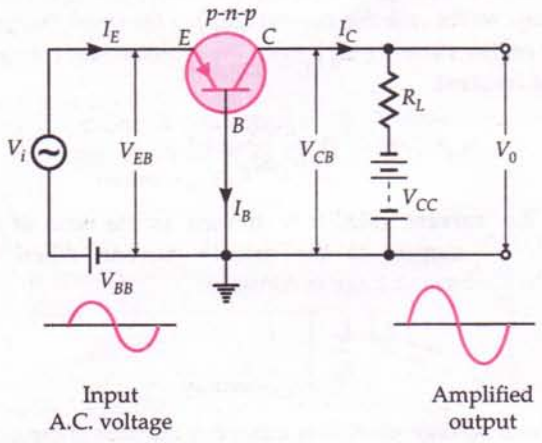


Fig. 14.73 *p-n-p* transistor as a common base amplifier.

The low input a.c. signal is superimposed on the forward bias V_{EB}. A load resistance R_L is connected between the collector and d.c. supply. The amplified output V_0 is obtained between collector and ground.

When no a.c. signal is fed to the input circuit, we have

$$I_E = I_B + I_C$$

When a current I_C flows in the circuit, voltage drop $I_C R_L$ occurs across the load R_L. The output voltage will be

$$V_0 = V_{CB} = V_{CC} - I_C R_L$$

When the input signal is applied in emitter base circuit, it changes the emitter-base voltage and the emitter current I_E. This, in turn, changes the collector current I_C and hence output voltage V_0 in accordance with the above relation. This variation in collector-base voltage appears as amplified output.

Phase relationship between input and output signals. When a.c. signal is fed to the input circuit, the positive half cycle increases the forward bias. This increases the emitter current and hence the collector current. The potential drop $I_C R_L$ across the load resistance increases. The collector voltage V_0 decreases. As collector is connected to the negative terminal of the battery V_{CC}, the decrease in collector voltage means that collector has become less negative or more positive. So, as the input a.c. signal goes through its positive half cycle, the output signal also goes through its positive half cycle. Similarly, as the input signal goes through its negative half cycle, the output signal also goes through its negative half cycle. Hence in common base amplifier, the input and output voltages are in same phase.

14.41 TRANSISTOR AS A COMMON EMITTER AMPLIFIER

47. *With the help of a labelled circuit diagram, explain the use of n-p-n transistor as a common emitter amplifier. Discuss phase relationship between input and output voltages. Write expressions for the various gains of a common emitter amplifier.*

n-p-n transistor as a common emitter amplifier. Figure 14.74 shows the use of *n-p-n* transistor as a common emitter amplifier. The emitter is common to both input and output circuits. The emitter is forward biased by battery V_{BB} and the collector is reverse biased by battery V_{CC}. This decreases the resistance R_{in} of the input circuit and increases the resistance R_{out} of the output circuit. The low a.c. input signal V_i is superimposed on the forward bias V_{BE}. A load resistance R_L is connected between the collector and the d.c. supply and the amplified output is obtained between the collector and the ground.

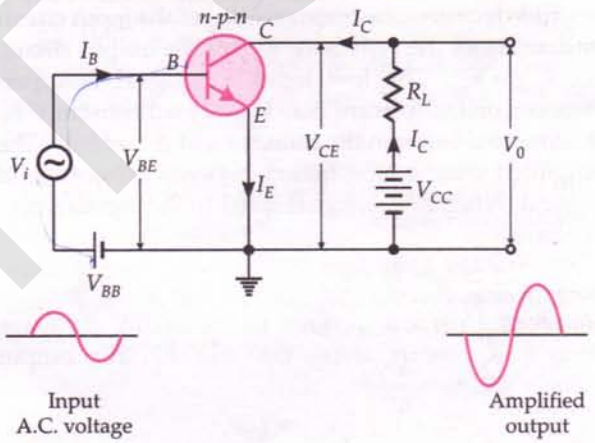


Fig. 14.74 *n-p-n* transistor as a common emitter amplifier.

When current I_C flows in the output circuit, the potential drop across the load resistance is $I_C R_L$. Hence the output voltage is

$$V_0 = V_{CE} = V_{CC} - I_C R_L$$

When the input signal is fed to the base-emitter circuit, the base-emitter voltage changes. This changes the emitter current I_E and hence the collector current I_C. The output voltage V_0 varies in accordance with the above relation. These variations in the collector voltage appear as amplified output.

Phase relationship between input and output signals. When an a.c. signal is fed to the input circuit, its positive half cycle increases the forward bias of the circuit which, in turn, increases the emitter current and hence the collector current. The increase in collector current increases the potential drop across R_L, which

makes the output voltage V_0 less positive or more negative. So as the input signal goes through its positive half cycle, the amplified output signal goes through a negative half cycle. Similarly, as the input signal goes through its negative half cycle, the amplified output signal goes through its positive half cycle. Hence *in a common emitter amplifier, the input and output voltages are 180° out of phase or in opposite phases.*

Current, voltage and power gains of a common emitter amplifier :

a.c. current gain. *It is defined as the ratio of the small change in the collector current* (ΔI_C) *to the small change in base current* (ΔI_B)*, when the collector-emitter voltage is kept constant.* It is denoted by β_{ac} or A_i. Thus

$$\beta_{ac} \quad \text{or} \quad A_i = \left[\frac{\Delta I_C}{\Delta I_B}\right]_{V_{CE} = \text{constant}}$$

d.c. current gain. *It is defined as the ratio of collector current to the base current, when collector-emitter voltage is constant.* Thus

$$\beta_{dc} = \left[\frac{I_C}{I_B}\right]_{V_{CE} = \text{constant}}$$

In the linear region of the output characteristics, β_{ac} is usually close to β_{dc}.

a.c. voltage gain. It is *defined as the ratio of small change in output voltage* (ΔV_{CE}) *to the small change in input voltage* (ΔV_{BE}). It is given by

$$A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

But $\Delta V_{BE} = R_i \cdot \Delta I_B$

where R_i is the resistance of the input or the emitter base circuit.

And $\Delta V_{CE} = -R_0 \cdot \Delta I_C$

where R_0 is the resistance of the output or collector-emitter circuit (including R_L). The –ve sign indicates that the input and output voltages have a phase difference of 180° *i.e.,* if the input voltage increases, the output voltage decreases.

$$\therefore \qquad A_v = -\frac{\Delta I_C}{\Delta I_B} \cdot \frac{R_{out}}{R_{in}} = -\beta_{ac} \cdot \frac{R_{out}}{R_{in}}$$

or $$A_v = A_i \cdot A_r$$

i.e., Voltage gain = Current gain × Resistance gain.

a.c. power gain. *It is defined as the small change in output power to the small change in input power.*

$$\text{a.c. power gain} = \frac{\text{Change in output power}}{\text{Change in input power}}$$

$$A_p = \frac{(\Delta I_C)^2 R_0}{(\Delta I_B)^2 R_i} = \beta_{ac}^2 \cdot \frac{R_0}{R_i}$$

As $\beta_{ac}^2 >> \alpha_{ac}^2$, the a.c. power gain of a common emitter amplifier is much larger than that of a common base amplifier. It may be noted that the transistor is not generating any power. The energy for the higher a.c. power at the output is supplied by the d.c. battery.

48. *With the help of a labelled circuit diagram, explain the use of p-n-p transistor as a common emitter amplifier. Discuss the phase relationship between input and output voltages.*

p-n-p transistor as a common emitter amplifier. Fig. 14.75 shows the use of *p-n-p* transistor as a common emitter amplifier. The emitter is common to both input and output circuits. The emitter is forward biased by battery V_{BB} while the collector is reverse biased by battery V_{CC}. This decreases the resistance R_{in} of the input circuit and increases the resistance R_{out} of the output circuit.

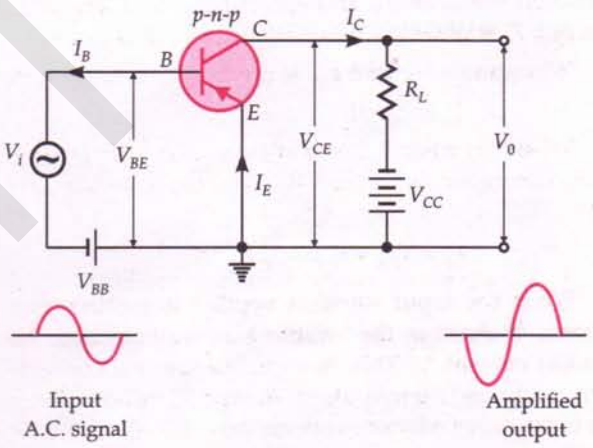


Fig. 14.75 *p-n-p* transistor as a common emitter amplifier.

The a.c. input signal V_i (to be amplified) is superimposed on the forward bias V_{BE}. A load R_L is connected between the collector and the d.c. supply and the amplified output is obtained between the collector and the ground. When current I_C flows in the output circuit, the potential drop across load resistance is $I_C R_L$.

Hence the output voltage is

$$V_0 = V_{CE} = V_{CC} - I_C R_L$$

When the input signal fed to the base-emitter circuit, the base-emitter voltage changes. This changes the emitter current I_E and hence the collector current I_C. The output voltage V_0 varies in accordance with the above relation. These variations in the collector voltage appear as amplified output.

Phase relationship between input and output signals. When a.c. is fed to the input circuit, its positive half cycle opposes the forward bias of emitter-base circuit. This decreases the emitter current and hence the collector current I_C. As a result, the collector voltage V_{CE} increases. As the collector is connected to the negative terminal of the battery V_{CC}, the increase in collector voltage means that the collector will become more negative. So as the input signal goes through its positive half cycle, the output signal goes through its negative half cycle. Similarly, as the input signal goes through its negative half cycle, the amplified output signal goes through its positive half cycle. So *in a common emitter amplifier, the input and output voltages are 180° out of phase.*

Examples Based on Transistor (i) Characteristics (ii) As an Amplifier

Formulae Used

1. $I_E = I_C + I_B$
2. For a common base transistor amplifier,
   (*i*) $\alpha_{dc} = \dfrac{I_C}{I_E}$ and $\alpha_{ac} = \dfrac{\Delta I_C}{\Delta I_E}$
   (*ii*) $A_v = \alpha_{ac} \cdot \dfrac{R_o}{R_i} = A_i \cdot A_r$
   (*iii*) $A_p = A_v \cdot A_i = \alpha_{ac}^2 \cdot \dfrac{R_o}{R_i}$
3. For a common emitter transistor amplifier,
   (*i*) $\beta_{dc} = \dfrac{I_C}{I_B}$ and $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B}$
   (*ii*) $A_v = A_i \cdot A_r = \beta_{ac} \cdot \dfrac{R_o}{R_i}$
   (*iii*) $A_p = A_v \cdot A_i = \beta_{ac}^2 \cdot \dfrac{R_o}{R_i}$
   (*iv*) $g_m = \dfrac{\Delta I_C}{\Delta V_{BE}}$
4. Relations between α and β are
   $\alpha = \dfrac{\beta}{1+\beta}$ and $\beta = \dfrac{\alpha}{1-\alpha}$

Units Used

Voltages are in volt, currents in ampere, g_m in Ω^{-1} or siemen (S), α and β have no units.

Example 22. *In p-n-p transistor circuit, the collector current is 10 mA. If 90% of the holes reach the collector, find emitter and base currents.* [IIT 92]

Solution. Here $I_E = 10$ mA. As 90% of the holes reach the collector, so the collector current,

$$I_C = 90\% \text{ of } I_E = \frac{90}{100} I_E$$

or $$I_E = \frac{100}{90} I_C = \frac{100}{90} \times 10 \simeq \mathbf{11\ mA.}$$

Base current, $I_B = I_E - I_C = 11 - 10 = \mathbf{1\ mA.}$

Example 23. *For a transistor connected in common emitter mode, the voltage drop across the collector is 2 V and β is 50. Find the base current, if R_C is 2 K.* [NCERT]

Solution. Here $V_{CE} = 2$ V, $\beta = 50$,

$$R_C = 2 \text{ K} = 2 \times 10^3\ \Omega$$

$$\therefore \quad I_C = \frac{V_{CE}}{R_C} = \frac{2}{2 \times 10^3} = 10^{-3} \text{ A} = \mathbf{1\ mA.}$$

As $$\beta = \frac{I_C}{I_B}$$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{10^{-3}}{50} \text{ A} = \mathbf{20\ \mu A}.$$

Example 24. *The potential difference across the collector of a transistor, used in common emitter mode is 1.5 V, with the collector resistance of 3 kΩ. Find (i) the emitter and (ii) the base current, if the d.c. gain of the transistor is 50.* [CBSE D 03C]

Solution. Here $V_{CE} = 1.5$ V,

$$R_C = 3\ \text{k}\Omega = 3 \times 10^3\ \Omega, \quad \beta = 50$$

$$\therefore \quad I_C = \frac{V_{CE}}{R_C} = \frac{1.5}{3 \times 10^3} = 0.50 \times 10^{-3} \text{ A}$$

$$I_B = \frac{I_C}{\beta} = \frac{0.50 \times 10^{-3}}{50} = 0.01 \times 10^{-3} \text{ A}$$

$$I_E = I_B + I_C = (0.01 + 0.50) \times 10^{-3} \text{ A}$$
$$= 0.51 \times 10^{-3} \text{ A} = \mathbf{0.51\ mA.}$$

Example 25. *The current gain for common emitter amplifier is 59. If the emitter current is 6.0 mA, find (i) base current (ii) collector current.* [CBSE D 03]

Solution. Here $\beta = 59$, $I_E = 6.0$ mA

Now $$\alpha = \frac{\beta}{1+\beta}$$

or $$\frac{I_C}{I_E} = \frac{59}{1+59}$$

or $$I_C = \frac{59}{60} I_E = \frac{59}{60} \times 6.0 = \mathbf{5.9\ mA}$$

$$I_B = I_E - I_C = 6.0 - 5.9 = \mathbf{0.1\ mA.}$$

Example 26. *A certain n-p-n transistor has the common emitter output characteristics as shown in Fig. 14.76.*

(*a*) *Find the emitter current at $V_{cc} = 10$ V and $I_b = 60\ \mu A$.*

(*b*) *Find β at this point..* **[CBSE Sample Paper 11]**

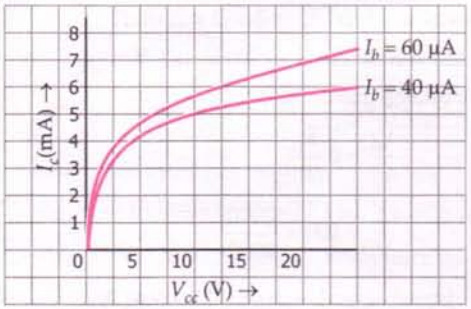


Fig 14.76

Solution. (*a*) For $V_{cc} = 10$ V and $I_b = 60\ \mu A$;

$$I_c = 6 \text{ mA}$$

$$I_e = I_c + I_b = 6 \text{ mA} + 60\ \mu A = \mathbf{6.06\ mA}.$$

$$(b)\ \beta = \frac{I_c}{I_b} = \frac{6 \text{ mA}}{60\ \mu A} = \mathbf{100}.$$

Example 27. *The input resistance of a transistor is 1000 Ω. On changing its base current by 10 μA, the collector current increases by 2 mA. If a load resistance of 5 kΩ is used in the circuit, calculate : (i) the current gain (ii) voltage gain of the amplifier* [CBSE. D 06]

Solution. Here,

$R_{in} = 1000\ \Omega$, $\Delta I_B = 10\ \mu A = 10^{-5}$ A

$R_{out} = 5\ k\Omega = 5 \times 10^3\ \Omega$, $\Delta I_C = 2 \text{ mA} = 2 \times 10^{-3}$ A

(*i*) Current gain,

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{2 \times 10^{-3}}{10^{-5}} = \mathbf{200}.$$

(*ii*) Voltage gain,

$$A_v = \beta \frac{R_{out}}{R_{in}} = \frac{200 \times 5 \times 10^3}{1000} = \mathbf{1000}.$$

Example 28. *Figure 14.77 shows the output characteristic of an n-p-n transistor in CE configuration. For this transistor, determine (i) the dynamic output resistance,*

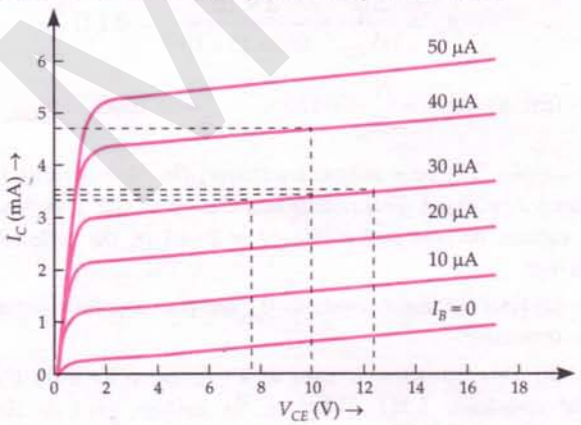


Fig. 14.77

(*ii*) *the dc current gain and* (*iii*) *the ac current gain; at an operating point* $V_{CE} = 10$ *V, when* $I_B = 30\ \mu A$. [CBSE D 13]

Solution. Draw a vertical line at $V_{CE} = 10$ V. The point of intersection of this line with the characteristic curve for $I_B = 30\ \mu A$ gives the operating point. At this point, $I_C = 3.6$ mA.

(*i*) To calculate the dynamic output resistance of the transistor, we consider a small change in V_{CE} around the operating point.

$$\therefore \quad R_{out} = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_E = 30\ \mu A} = \frac{12.5 - 7.5}{(3.7 - 3.5) \times 10^{-3}}$$

$$= 25 \times 10^3\ \Omega = \mathbf{25\ k\ \Omega}$$

(*ii*) From the output characteristic, when $I_B = 30\ \mu A$, we have $I_C = 3.6$ mA. Therefore, the dc current gain is

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{3.6 \text{ mA}}{30\ \mu A} = \mathbf{120}.$$

(*iii*) To determine ac current gain, we draw a vertical line corresponding to $V_{CE} = 10$ V. Then from the output characteristic, the ac current gain is

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = 10 \text{ V}} = \frac{(4.7 - 3.6) \text{ mA}}{(40 - 30)\ \mu A}$$

$$= \frac{1.1 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{110}.$$

Example 29. *Calculate the input resistance of the transistor operating at* $V_{CE} = 4$ *V in CE configuration having its input characteristics as shown in Fig. 14.67.* [NCERT]

Solution. Consider the input characteristic corresponding to $V_{CE} = 4$ V. Then from the dashed lines drawn to this curve, we get

$$\Delta V_{BE} = (1.1 - 0.9) \text{ V} = 0.2 \text{ V}$$

$$\Delta I_B = (68 - 34)\ \mu A = 34 \times 10^{-6} \text{ A}$$

$$R_{in} = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}} = \frac{0.2 \text{ V}}{34 \times 10^{-6} \text{ A}} \simeq \mathbf{6000\ A}.$$

Example 30. *From the output characteristics shown in Fig. 14.68, calculate the value of current amplification factor of the transistor when* V_{CE} *is 2 V.*

Solution. Consider two output characteristics corresponding to $I_B = 10\ \mu A$ and $I_B = 60\ \mu A$. Then for $V_{CE} = 2$ V, from these curves, we get

$$\Delta I_B \simeq (60 - 10)\ \mu A = 50\ \mu A = 50 \times 10^{-6} \text{ A}$$

$$\Delta I_C \simeq (9.5 - 2.5) \text{ mA} = 7.0 \text{ mA} = 7.0 \times 10^{-3} \text{ A}$$

$$\therefore \quad \beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}} = \left(\frac{7 \times 10^{-3} \text{ A}}{50 \times 10^{-6} \text{ A}}\right) = \mathbf{40}.$$

Example 31. *For a CE-transistor amplifier, the audio signal voltage across the collector resistance of 2.0 kΩ is 2.0 V. Suppose the current amplification factor of the transistor is 100, what should be the value of R_B in series with V_{BB} supply of 2.0 V if the dc base current has to be 10 times the signal current ? Also calculate the dc drop across the collector resistance. Take $V_{BE} = 0.6$ V.* [NCERT]

Solution. Here $R_C = 2.0\ \text{k}\Omega$, $\beta = 100$, $V_{BB} = 2.0$ V, $V_{BE} = 0.6$ V

The output ac voltage = 2.0 V

∴ The ac collector current,

$$i_C = \frac{2.0\ \text{V}}{R_C} = \frac{2.0\ \text{V}}{2.0 \times 10^3\ \Omega} = 1.0\ \text{mA}$$

The signal current through the base,

$$i_B = \frac{i_C}{\beta} = \frac{1.0\ \text{mA}}{100} = 0.010\ \text{mA}$$

The dc base current,

$$I_B = 10 \times \text{signal current}$$
$$= 10 \times 0.010 = 0.10\ \text{mA}$$
$$R_B = \frac{V_{BB} - V_{EB}}{I_B} = \frac{(2.0 - 0.6)\ \text{V}}{0.10\ \text{mA}} = \mathbf{14\ k\Omega}$$

The dc collector current,

$$I_C = \beta I_B = 100 \times 0.10\ \text{mA} = 10\ \text{mA}$$

The dc drop across the collector resistance

$$= I_C R_C = 10\ \text{mA} \times 2.0\ \text{k}\Omega = \mathbf{20\ V}.$$

Example 32. *A transistor has a current amplification factor (current gain) of 50. In a CE-amplifier circuit, the collector resistance is chosen as 5 Ω and the input resistance is 1 Ω. Calculate the output voltage if input voltage is 0.01 V.* [NCERT]

Solution. Here $\beta = 50$, $R_C = 5\ \text{k}\Omega = 5 \times 10^3\ \Omega$,

$R_B = 1\ \text{k}\Omega = 1 \times 10^3\ \Omega$, $V_i = 0.01$ V, $V_0 = ?$

The voltage gain of a common emitter amplifier

$$A_v = \beta \frac{R_0}{R_i}$$

or
$$\frac{V_0}{V_i} = \beta . \frac{R_C}{R_B}$$

∴
$$V_o = \frac{\beta R_C V_i}{R_B} = \frac{50 \times 5 \times 10^3 \times 0.01}{1 \times 10^3} = \mathbf{2.5\ V}.$$

Example 33. *For a common emitter transistor amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 2 V. If the current amplification factor of the transistor is 100, calculate (i) input signal voltage, (ii) base current, and (iii) power gain. Given that the value of the base resistance is 1 kΩ.* [CBSE D 05 C ; NCERT]

Solution. Here $R_C = 2\ \text{k}\Omega = 2000\ \Omega$,

$R_B = 1\ \text{k}\Omega = 1000\ \Omega$, $\beta = 100$, $V_0 = 2$ V

(*i*) Voltage gain,

$$\frac{V_0}{V_i} = \beta \frac{R_0}{R_i}$$

or
$$\frac{2}{V_i} = 100 \times \frac{2000}{1000}$$

∴ Input signal voltage, $V_i = \mathbf{0.01\ V}$.

(*ii*) $\beta = \frac{I_C}{I_B} = \frac{V_0 / R_C}{I_B}$

∴ Base current,

$$I_B = \frac{V_0}{\beta R_C} = \frac{2}{100 \times 2000}$$
$$= 10^{-5}\ \text{A} = \mathbf{10\ \mu A}.$$

(*iii*) Power gain = $\beta^2 \frac{R_0}{R_i} = (100)^2 \times \frac{200}{1000} = \mathbf{2000}$.

Example 34. *The input resistance of a silicon transistor is 665 Ω. Its base current is changed by 15 μA which results in the change in collector current by 2 mA. This transistor is used as a common emitter amplifier with a load resistance of 5 kΩ. Calculate :*

(*i*) *current gain '$\beta_{a.c.}$',*

(*ii*) *trans-conductance 'g_m' and*

(*iii*) *voltage gain 'A_v' of the amplifier.* [CBSE OD 01C]

Solution. Here $R_{in} = 665\ \Omega$,

$$R_{out} = 5\ \text{k}\Omega = 5 \times 10^3\ \Omega,$$

(*i*) $\beta_{\text{a.c.}} = \frac{\Delta I_C}{\Delta I_B} = \frac{2\ \text{mA}}{15\ \mu\text{A}} = \frac{2 \times 10^{-3}\ \text{A}}{15 \times 10^{-6}\ \text{A}} = \mathbf{133}.$

(*ii*) As $R_{in} = \frac{\Delta V_{EB}}{\Delta I_B}$

∴ $\Delta V_{EB} = R_{in} \times \Delta I_B = 665 \times 15 \times 10^{-6}\ \text{V}$

∴ $g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{2 \times 10^{-3}}{665 \times 15 \times 10^{-6}} = \mathbf{0.2\ \Omega^{-1}}.$

(*iii*) $A_v = \beta_{\text{a.c.}} \times \frac{R_{out}}{R_{in}} = 133 \times \frac{5 \times 10^3}{665} = \mathbf{1000}.$

Example 35. *In a silicon transistor, the base current is changed by 20 μA. This results in a change of 0.02 V in base to emitter voltage and a change of 2 mA in the collector current.*

(*a*) *Find the input resistance β_{ac} and transconductance of the transistor.*

(*b*) *This transistor is used as a CE amplifier with the load resistance 5 kΩ. What is the voltage gain of the amplifier ?* [CBSE OD 01C]

Solution. Here $\Delta I_B = 20\ \mu A = 20 \times 10^{-6}$ A

$\Delta I_C = 2$ m A $= 2 \times 10^{-3}$ A, $\Delta V_{BE} = 0.02$ V

(*a*) Input resistance,

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{0.02}{20 \times 10^{-6}}\ \Omega = \mathbf{1000\ \Omega}$$

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{2 \times 10^{-3}}{20 \times 10^{-6}} = \mathbf{100}$$

Transconductance,

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{2 \times 10^{-3}}{0.02}\ \Omega^{-1} = \mathbf{0.1\ \Omega^{-1}}$$

(*b*) Load resistance, $R_L = 5\ k\Omega = 5 \times 10^3\ \Omega$

$\therefore$ Voltage gain ,

$$A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}} = \frac{R_L . \Delta I_C}{\Delta V_{BE}}$$

$$= \frac{5 \times 10^3 \times 2 \times 10^{-3}}{0.02} = \mathbf{500.}$$

Example 36. *An n-p-n transistor is connected in common-emitter configuration in which collector supply is 8 V and the voltage-drop across the load-resistance of 800 Ω connected in the collector circuit is 0.8 V. If current amplification factor is 25, determine collector-emitter voltage and base-current. If the internal resistance of the transistor is 200 Ω, calculate the voltage-gain and power-gain.*

[Roorkee 94]

Solution. A common-emitter *n-p-n* amplifier circuit is shown in Fig. 14.78. Here V_{CC} and V_{BB} are the collector-supply and base-supply voltages respectively and R_L is the load-resistance in the collector circuit.

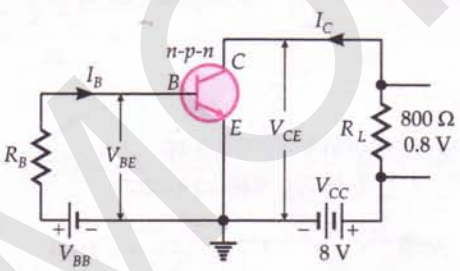


Fig. 14.78

Collector current,

$$I_C = \frac{\text{Voltage - drop across } R_L}{R_L}$$

$$= \frac{0.8}{800} = 1.0 \times 10^{-3}\ \text{A}$$

Collector-emitter voltage,

$$V_{CE} = V_{CC} - I_C\ R_L = 8 - 0.8 = 7.2\ \text{V}$$

As $\beta = \dfrac{I_C}{I_B}$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{1.0 \times 10^{-3}\ \text{A}}{25} \qquad [\because \beta = 25]$$

$$= 0.04 \times 10^{-3}\ \text{A} = 40\ \mu\text{A}.$$

Voltage gain, $A_v = \beta . \dfrac{R_L}{R_B} = 25 \times \dfrac{800}{200} = \mathbf{100}$

Power gain, $A_p = \beta^2 . \dfrac{R_L}{R_B} = (25)^2 \times \dfrac{800}{200} = \mathbf{2500.}$

Example 37. *In the circuit shown in Fig. 14.79, the value of β is 100. Find I_B, V_{CE}, V_{BE} and V_{BC}, when $I_C = 1.5$ mA. The transistor is in active, cut off or saturation state ?*

[NCERT]

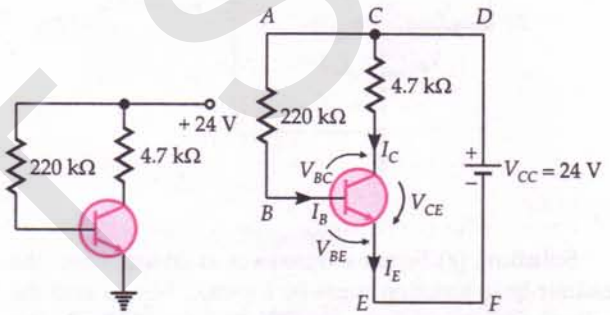


Fig. 14.79 Fig. 14.80

Solution. Figure 14.80 shows the equivalent circuit of the given circuit.

Here

$\beta = 100$, $I_C = 1.5$ mA $= 1.5 \times 10^{-3}$ A, $V_{CC} = 24$ V

As $\beta = \dfrac{I_C}{I_B}$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{1.5 \times 10^{-3}}{100}\ \text{A} = \mathbf{15\ \mu A.}$$

To calculate V_{CE}, we apply Kirchhoff's rule to loop *CEFDC*, therefore

$$V_{CC} = I_C \times 4.7\ \text{k}\Omega + V_{CE}$$

or $$24 = 1.5 \times 10^{-3} \times 4.7 \times 10^3 + V_{CE}$$

or $$V_{CE} = 24 - 7.05 = \mathbf{16.95\ V}$$

Again, applying Kirchhof's rule to loop *ABEFDCA*, we get

$$V_{CC} = I_B \times 220\ \text{k}\Omega + V_{BE}$$

or $$24 = 15 \times 10^{-6} \times 220 \times 10^{-3} + V_{BE}$$

$\therefore$ $$V_{BE} = 24 - 3.3 = \mathbf{20.7\ V.}$$

Going along loop *ABCA*, we get

$$I_B \times 220\ \text{k}\Omega + V_{BC} = I_C \times 4.7\ \text{k}\Omega$$

or $$15 \times 10^{-6} \times 220 \times 10^3 + V_{BC} = 1.5 \times 10^{-3} \times 4.7 \times 10^3$$

$$\therefore \quad V_{BC} = 7.05 - 3.3 = \mathbf{3.75\ V}$$

As $V_{CE} < V_{BE}$, both the junctions are forward biased. So the transistor is in the saturation state.

Example 38. *In the circuit shown in Fig. 14.81, the base current I_B is 10 μA and the collector current is 5.2 mA. (a) Can this transistor circuit be used as an amplifier ? (b) What happens if the resistance R_C is 500 Ω and I_B, I_C and R_B remain same as above ?*

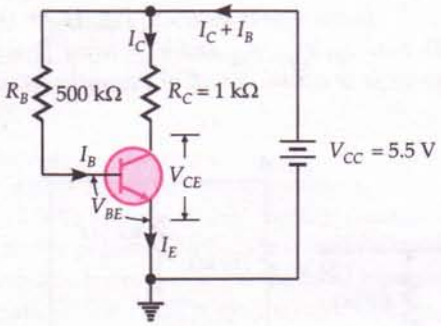


Fig. 14.81

Solution. (*a*) To use a transistor as an amplifier, the emitter-base junction must be forward biased and the collector-base junction must be reverse biased. We now determine V_{BE} and V_{CE}.

Applying Kirchhoff's law to the loop containing the base resistor and emitter-base junction, we get

$$V_{CC} = V_{BE} + I_B R_B$$

i.e., $$V_{BE} = V_{CC} - I_B R_B$$

$$= 5.5\ \text{V} - 10 \times 10^{-6} \times 5 \times 10^{-5}\ \text{V} = 0.5\ \text{V}$$

Applying Kirchhoff's law to the collector-emitter loop, we get

$$V_{CC} = V_{CE} + I_C R_C$$

i.e., $$V_{CE} = V_{CC} - I_C R_C$$

$$= (5.5 - 5.2 \times 10^{-3} \times 1 \times 10^3)\ \text{V}$$

$$= (5.5 - 5.2)\ \text{V} = 0.3\ \text{V}$$

The collector is found to be at + 0.3 V with respect to the emitter and the base is at + 0.5 V with respect to the emitter, so the base is at + 0.2 V with respect to the collector. Thus, both the emitter-base and collector-base junctions are forward biased. Hence, the circuit cannot be used as an amplifier.

(*b*) When the resistance R_C of 500 Ω is used, the voltage of collector with respect to emitter is

$$V_{CE} = (5.5 - 5.2 \times 10^3 \times 500)\ \text{V}$$

$$= (5.5 - 2.60)\ \text{V} = \mathbf{2.9\ V}$$

Now the collector is at 2.9 V with respect to emitter and base is at 0.5 V with respect to emitter. So the base collector junction is reverse biased by −2.4 V. Hence the circuit can now work as an amplifier.

Example 39. *In the circuit shown in Fig. 14.82, if we assume that when the input voltage at the base resistance is 5 V, V_{BE} is zero and V_{CE} is also zero ; what is I_B, I_C and β ? When the input is zero, the I_B is zero. What will be the output waveform if the input waveform is as shown in Fig. 14.82 ?* [NCERT]

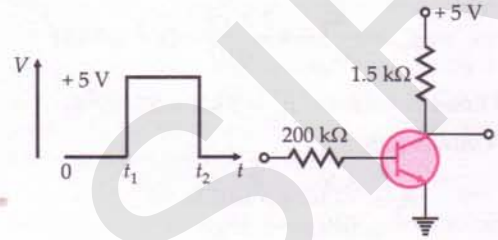


Fig. 14.82

Solution. Various voltages and resistances are shown in Fig. 14.83(*a*).

Here $R_B = 200\ \text{k}\Omega$, $V_{BE} = 0$

$V_{CE} = 0$, $V_{BB} = +5\ \text{V}$,

$V_{CC} = +5\ \text{V}$, $R_C = 1.5\ \text{k}\Omega$

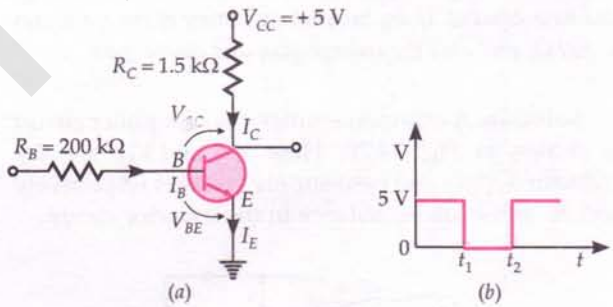


Fig. 14.83

Using Kirchhoff's second rule,

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{5 - 0}{1.5 \times 10^3}$$

$$= 3.3 \times 10^{-3}\ \text{A} = \mathbf{3.3\ mA}$$

$$I_B = \frac{\text{Base voltage}}{\text{Base resistance}} = \frac{V_{BB}}{R_B} = \frac{5}{200 \times 10^3}\ \text{A}$$

$$= 25 \times 10^{-6}\ \text{A} = \mathbf{25\ \mu\ A}$$

$$\beta = \frac{I_C}{I_B} = \frac{3.3 \times 10^{-3}}{25 \times 10^{-6}\ \text{A}} = \mathbf{133.3}$$

Since a *CE* configuration of a transistor inverts the input signal, so the output waveform is of the type shown in Fig. 14.83(*b*).

Example 40. *An amplifier is represented by the circuit shown in Fig. 14.84, r_i is the input resistance of the amplifier and the voltage v_i is appearing across it. This voltage is amplified by a factor of A_v and appears across the load as voltage v_0.*

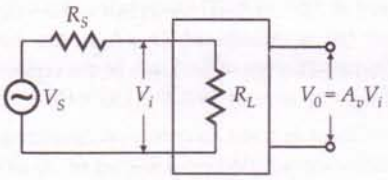


Fig. 14.84

An external voltage v_s is applied at the input terminals of the amplifier via series resistor R_s. What will be the apparent gain $A'_v = v_0 / v_s$ of the amplifier ? Express the gain in terms of A_v, R_s and r_i.

Solution. Voltage gain, $A_v = \dfrac{v_0}{v_i}$

As v_s is the voltage of the source, therefore, the voltage across the input terminals of the amplifier is

$$v_i = \frac{v_s \cdot r_i}{r_i + R_s} \quad \therefore \quad A_v = \frac{v_0}{v_i} = \frac{v_0(r_i + R_s)}{v_s\, r_i}$$

Hence the voltage gain,

$$A'_v = \frac{v_0}{v_s} = \frac{r_i}{R_s + r_i} A_v .$$

Example 41. *Figure 14.84 represents an amplifier circuit with an input internal resistance $r_i = 50\ k\,\Omega$. It is connected to an ac voltage source through a series resistor of 100 kΩ. The no load voltage gain of the transistor is 100. What is the apparent gain of the amplifier ?*

Solution. Voltage gain,

$$A_v = \frac{v_o}{v_i} = 100 \quad \therefore \quad v_0 = 100\, v_i$$

If v_s is the voltage of the source, then voltage across the input of the amplifier is

$$v_i = \frac{v_s \times r_i}{r_i + R_s} \quad \therefore \quad v_s = \frac{(r_i + R_s)v_i}{r_i}$$

∴ The apparent gain of the amplifier is

$$A'_v = \frac{v_0}{v_s} = \frac{100\, v_i}{\dfrac{(r_i + R_s)v_i}{r_i}} = \frac{100\, r_i}{r_i + R_s}$$

$$= \frac{100 \times 50 \times 10^3}{(50 + 100) \times 10^3} = \frac{100}{3} = \mathbf{33.33.}$$

Example 42. *In the circuit, shown in Fig. 14.85, $v_s = 0.2\ V$, $v_0 = -10\ V$. Find v_i and gain $A_v = v_0 / v_i$ and $A'_v = v_0 / v_s$.*

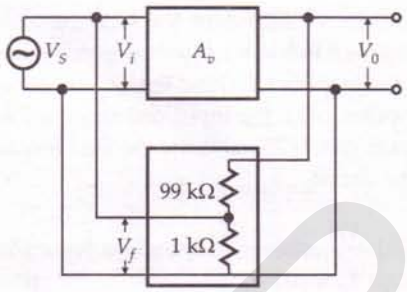


Fig. 14.85

Solution. $v_s = 0.2$ V, $v_0 = -10$ V

$$v_f = \frac{1}{99+1} v_0 = \frac{1}{100} \times (-10) = \mathbf{-0.1\ V}$$

$$v_i = v_s - v_f = 0.2 - (-0.1) = \mathbf{0.3\ V}$$

Also $v_i = v_s + v_f = 0.2 + (-0.1) = 0.1$ V

$$\therefore \text{ Gain, } A_v = \frac{v_0}{v_i} = \frac{-10}{0.1} = \mathbf{-100}$$

$$A'_v = \frac{v_0}{v_s} = \frac{-10}{0.2} = \mathbf{-50.}$$

Problems For Practice

1. In a common emitter transistor circuit, if the collector-emitter voltage changes by 0.2 V, the collector current changes by 0.004 mA. What is the output resistance of the circuits. (Ans. 50 kΩ)
2. If a change of 100 μA in the base current of an *n-p-n* transistor causes a change of 10 mA in its collector current, what is its a.c. current gain ? **[CBSE F 94C]** (Ans. 100)
3. The ac current gain of a transistor is 120. What is the change in the collector current in the transistor whose base current changes by 100 μA ? **[CBSE D 06C]** (Ans. 12 mA)
4. A transistor has a current gain of 30. If the collector resistance is 6 kΩ, input resistance is 1 kΩ, calculate its voltage gain. **[CBSE D 98C]** (Ans. 180)
5. In a transistor connected in common emitter mode, $R_C = 4$ K, $R_i = 1$ K, $I_C = 1$ mA and $I_B = 20$ μA. Find the voltage gain. (Ans. 200)
6. In a transistor amplifier, $\beta = 62$, $R_L = 5000\,\Omega$ and internal resistance of the transistor $= 500\,\Omega$. Calculate the voltage amplification and power amplification. (Ans. 620, 38 440)
7. A transistor has $\alpha = 0.95$. If the emitter current is 10 mA, what is (*a*) the collector current, (*b*) the base current, and (*iii*) gain β ? [Ans. (*a*) 9.5 mA (*b*) 0.5 mA (*c*) 19]

8. A change of 0.2 mA in the base current causes a change of 5 mA in the collector current for a common emitter amplifier. (*i*) Find the a.c. current gain of the transistor. (*ii*) If the input resistance is 2 kΩ and its voltage gain is 75, calculate the load resistance used in the circuit. **[CBSE F 04]**

[Ans. (*i*) 25 (*ii*) 6 kΩ]

9. Calculate emitter current for which β = 100 and base current $I_B = 20\,\mu A$. **[Himachal 02]**

(Ans. 2.02 mA)

10. The input resistance of a common-emitter amplifier is 2 kΩ and a.c. current gain is 20. If the load resistor used is 5 kΩ, calculate (*i*) the voltage gain of the amplifier, and (*ii*) the transconductance of the transistor used. **[CBSE OD 99]**

(Ans. 50, $0.01\,\Omega^{-1}$)

11. The input resistance, in the common emitter amplifier circuit of a given transistor, has a value of 1.5 kΩ. The output of this circuit, is obtained across a collector resistance of 7.5 kΩ. What would be the output voltage, corresponding to an input voltage of 5 mV, if the current amplification factor, of this transistor, has a value of 60 ? **[CBSE D 04C]**

(Ans. 1.5 V)

12. The current gain of a transistor in common base arrangement is 0.95. Find the voltage gain and power gain if load resistance of output circuit is 400 kΩ and input resistance is 200 Ω. **[Himachal 04]**

(Ans. 1900, 1805)

13. In common emitter amplifier, current gain is 60. If the emitter current is 7.7 mA, calculate the base current and collector current. Also calculate current gain, when the same transistor is working as common base amplifier. **[Punjab 01]**

(Ans. 0.126 mA, 7.574 mA, 0.984)

14. The power gain for *CB* amplifier is 800, and the voltage amplification factor is 840. Find the collector current when the base current is 1.2 mA.

(Ans. 24 mA)

15. The current gain of a transistor in *CB* configuration is 0.98. Find the change in collector current corresponding to a change of 5.0 mA in the emitter current. What would be the change in base current ? (Ans. 4.9 mA, 0.1 mA)

16. In common-emitter transistor amplifier, the load resistance of the output circuit is 1000 times the load resistance of the input circuit. If α = 0.98, then calculate the voltage gain. (Ans. 49×10^3)

17. In a common-emitter transistor amplifier, an increase of 50 μA in the base current causes an increase of 1.0 mA in the collector current. Calculate gain β. What will be the change in emitter current ? Also calculate current gain α.

(Ans. 20, 1050 μA, $\frac{20}{21}$)

18. The base current of a transistor is 105 μA and collector current is 2.05 mA. (*i*) Determine the value of β, I_E and α. (*ii*) A change of 27 μA in the base current produces a change of 0.65 mA in the collector current. Find β_{ac}. [Ans. (*i*) 19.52, 2.155 mA, 0.95 (*ii*) 24.07]

19. A transistor is used in common emitter mode in an amplifier circuit. When a signal of 30 mV is added to the base-emitter voltage, the base current changes by 30 μA and collector current by 3 mA. The load resistance is 5 kΩ. Calculate (*i*) the current gain β (*ii*) the input resistance R_{BE} (*iii*) transconductance and (*iv*) voltage gain.

[Ans. (*i*) 100 (*ii*) 1000 Ω (*iii*) $0.1\,\Omega^{-1}$ (*iv*) 500]

20. In the circuit shown in Fig. 14.86, the base current $I_B = 5.0\,\mu A$, base resistor $R_B = 1.0\,M\Omega$, collector resistor $R_C = 1.1\,k\Omega$, the collector current $I_C = 5.0$ mA and the d.c. voltage in the collector circuit $V_{CC} = 6.0$ V. (*i*) Can this circuit be used as an amplifier ? (*ii*) What happens if the resistance R_C is 400 Ω and I_B, I_C and R_B remain same as above ?

[Ans. (*i*) No (*ii*) can be used as amplifier]

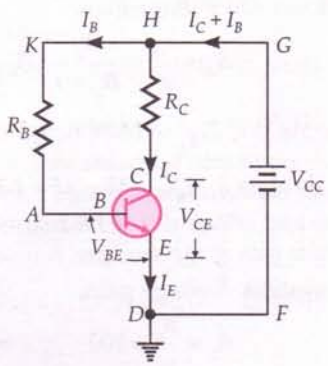


Fig. 14.86

21. As shown in Fig. 14.84, an amplifier of no load gain 400 and input resistance 100 Ω is connected to external signal via a series resistance of 300 Ω. What is the apparent voltage gain ? (Ans. 100)

HINTS

1. Here $\Delta V_{CE} = 0.2$ V, $\Delta I_C = 0.004\,mA = 4 \times 10^{-6}\,A$

Output resistance,

$$R_o = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{0.2}{4 \times 10^{-6}} = 50 \times 10^3\,\Omega = \mathbf{50\ k\Omega}.$$

2. Here $\Delta I_B = 100\,\mu A = 100 \times 10^{-6}$ A,

$\Delta I_C = 10\,mA = 10 \times 10^{-3}$ A

∴ a.c. current gain,

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{10 \times 10^{-3}}{100 \times 10^{-6}} = \mathbf{100}.$$

3. Here $\Delta I_B = 100\,\mu A = 100 \times 10^{-6}\,A$,
$\beta_{ac} = 120$, $\Delta I_C = ?$
As $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B}$ $\therefore$ $120 = \dfrac{\Delta I_C}{100 \times 10^{-6}}$
$\therefore$ Change in collector current,
$\Delta I_C = 120 \times 100 \times 10^{-6} = 12 \times 10^{-3}\,A = \mathbf{12\ mA}$.

4. Voltage gain = Current gain × Resistance gain
$= \text{Current gain} \times \dfrac{R_C}{R_i} = 30 \times \dfrac{6}{1} = \mathbf{180}.$

5. Voltage gain,
$$A_v = \beta \cdot \frac{R_C}{R_i} = \frac{I_C}{I_B} \cdot \frac{R_C}{R_i}$$
$$= \frac{1 \times 10^{-3} \times 4 \times 10^3}{20 \times 10^{-6} \times 1 \times 10^3} = \mathbf{200}.$$

6. Here $\beta = 62$, $R_L = 5000\,\Omega$, $R_{in} = 500\,\Omega$
The voltage amplification,
$$A_v = \beta \cdot \frac{R_{out}}{R_{in}} \simeq \beta \cdot \frac{R_L}{R_i} = 62 \times \frac{5000}{500} = \mathbf{620}$$
$[\because R_L \simeq R_{out}]$
The power gain,
$$A_p = \beta^2 \cdot \frac{R_{out}}{R_{in}} = (62)^2 \times \frac{5000}{500} = \mathbf{38{,}440}.$$

7. Here $\alpha = 0.95$, $I_E = 10$ mA
(*a*) As $\alpha = \dfrac{I_C}{I_E}$ $\therefore$ $I_C = \alpha\, I_E = 0.95 \times 10 = \mathbf{9.5\ mA}$.
(*b*) $I_B = I_E - I_C = 10 - 9.5 = \mathbf{0.5\ mA}$.
(*c*) $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.95}{1-0.95} = \dfrac{0.95}{0.05} = \mathbf{19}$.

8. Here $\Delta I_B = 0.2$ mA, $\Delta I_C = 5$ mA
(*i*) $\beta = \dfrac{\Delta I_C}{\Delta I_B} = \dfrac{5\ \text{mA}}{0.2\ \text{mA}} = \mathbf{25}.$
(*ii*) As $A_v = \beta \dfrac{R_L}{R_i}$
$\therefore$ $R_L = \dfrac{A_v R_i}{\beta} = \dfrac{75 \times 2\text{k}\Omega}{25} = \mathbf{6\ k\Omega}.$

9. $\beta = \dfrac{I_C}{I_B} = \dfrac{I_E - I_B}{I_B}$ or $100 = \dfrac{I_C - 20}{20}$
or $I_C = 2020\,\mu A = \mathbf{2.02\ mA}$.

10. (*i*) Voltage gain $= \beta_{ac} \times \dfrac{R_{out}}{R_{in}} = 20 \times \dfrac{5 \times 10^3}{2 \times 10^3} = \mathbf{50}.$
(*ii*) Transconductance,
$$g_m = \frac{\beta}{R_{in}} = \frac{20}{2 \times 10^3} = \mathbf{0.01\,\Omega^{-1}}.$$

11. $A_v = \dfrac{V_0}{V_i} = \beta \dfrac{R_C}{R_B}$
or $V_0 = \beta \dfrac{R_C V_i}{R_B} = \dfrac{60 \times 7.5 \times 10^3 \times 5 \times 10^{-3}}{1.5 \times 10^3} = \mathbf{1.5\ V}.$

12. Voltage gain $= \alpha \cdot \dfrac{R_0}{R_i} = 0.95 \times \dfrac{400 \times 10^3}{200} = \mathbf{1900}.$
Power gain = Voltage gain × Current gain
$= 1900 \times 0.95 = \mathbf{1805}.$

13. $\beta = \dfrac{I_C}{I_B} = \dfrac{I_E - I_B}{I_B}$ or $60 = \dfrac{7.7 - I_B}{I_B}$
or $I_B = \mathbf{0.126\ mA}$.
Also, $I_C = I_E - I_B = 7.7 - 0.126 = \mathbf{7.574\ mA}$.
$\alpha = \dfrac{\beta}{1+\beta} = \dfrac{60}{1+60} = \mathbf{0.984}.$

14. Current gain, $\alpha = \dfrac{\text{Power gain}}{\text{Voltage gain}} = \dfrac{800}{840} = \dfrac{20}{21}$
Now $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{20/21}{1 - 20/21} = 20$
But $\beta = \dfrac{I_C}{I_B}$ $\therefore$ $I_C = \beta \cdot I_B = 20 \times 1.2 = \mathbf{24\ mA}$

15. $\Delta I_C = \alpha \cdot \Delta I_E = 0.98 \times 5.0\ \text{mA} = \mathbf{4.9\ mA}$.
$\Delta I_B = \Delta I_E - \Delta I_C = 5.0 - 4.9 = \mathbf{0.1\ mA}$.

16. $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.98}{1 - 0.98} = 49$
Voltage gain $= \beta \cdot \dfrac{R_0}{R_i} = 49 \times 1000 = \mathbf{49 \times 10^3}.$

17. $\beta = \dfrac{\Delta I_C}{\Delta I_B} = \dfrac{1.0 \times 10^{-3}\ A}{50 \times 10^{-6}\ A} = \mathbf{20}.$
$\Delta I_E = \Delta I_B + \Delta I_C = 50 \times 10^{-6} + 1.0 \times 10^{-3}$
$= 1050 \times 10^{-6}\,A = \mathbf{1050\,\mu A}.$
$\alpha = \dfrac{\beta}{1+\beta} = \dfrac{20}{1+20} = \mathbf{\dfrac{20}{21}}.$

18. (*i*) $I_E = I_B + I_C = 105 \times 10^{-6} + 2.05 \times 10^{-3}$
$= 2.155 \times 10^{-3}\,A = \mathbf{2.155\ mA}.$
$\beta = \dfrac{I_C}{I_B} = \dfrac{3.05 \times 10^{-3}}{105 \times 10^{-6}} = \mathbf{19.52}$,
$\alpha = \dfrac{I_C}{I_E} = \dfrac{2.05 \times 10^{-3}}{2.155 \times 10^{-3}} = \mathbf{0.95}.$
(*ii*) $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B} = \dfrac{0.65 \times 10^{-3}}{27 \times 10^{-6}} = \mathbf{24.07}.$

19. (*i*) $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B} = \dfrac{3 \times 10^{-3}\ A}{30 \times 10^{-6}\ A} = \mathbf{100}.$
(*ii*) Input resistance,
$$R_{BE} = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{30\ \text{mV}}{30\,\mu A} = \mathbf{1000\,\Omega}.$$

(*iii*) Transconductance,

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{3\text{ mA}}{30\text{ mV}} = 0.1\,\Omega^{-1} \text{ or S.}$$

(*iv*) Output voltage,

$$V_0 = R_L \,.\, \Delta I_C = 5\text{ k}\Omega \times 3\text{ mA} = \mathbf{15\text{ V}}.$$

$$\text{Voltage gain} = \frac{V_0}{V_i} = \frac{15\text{ V}}{30\text{ mV}} = \mathbf{500}.$$

20. (*i*) Applying Kirchhoff's second law to the loop *ABEDFGHKA*, we get

$$V_{CC} = V_{BE} + I_B R_B$$

or $$V_{BE} = V_{CC} - I_B R_B$$

$$= 6.0 - 5.0 \times 10^{-6} \times 1.0 \times 10^6 = 1.0\text{ V}$$

Applying Kirchhoff's second law to the loop *EDFGHCBE*, we get

$$V_{CC} = V_{CE} + I_C R_C$$

or $$V_{CE} = V_{CC} - I_C R_C$$

$$= 6.0 - 5.0 \times 10^{-3} \times 1.1 \times 10^3 = 0.5\text{ V}.$$

The collector is at + 0.5 V w.r.t. the emitter and the base is + 1.0 V w.r.t. emitter, so the base is at (1.0 – 0.5) = + 0.5 V w.r.t. the collector. Thus, both the emitter-base and collector-base junctions are forward biased. Hence the circuit cannot be used as an amplifier.

(*ii*) When $R_C = 400\,\Omega$,

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 6.0 - 5.0 \times 10^{-3} \times 400 = 4.0\text{ V}.$$

Now the collector is at + 4.0 V w.r.t. the emitter and the base is at + 1.0 V w.r.t. the emitter. Thus, the base-collector is reversed biased by (1.0 – 4.0) = – 3.0 V. Hence the circuit can now work as an amplifier.

21. Apparent voltage gain,

$$A_v' = \frac{r_i}{R_s + r_i} \,.\, A_v = \frac{100}{300 + 100} \times 400 = \mathbf{100}.$$

14.42 TRANSISTOR AS AN OSCILLATOR*

49. *What is an oscillator ? Give its working principle. With the help of labelled circuit diagram, explain how a transistor can be used to produce self-sustained oscillations.*

Oscillator. An *oscillator is an electronic device which produces electric oscillation of constant frequency and amplitude, without requiring any external input signal.* It converts dc energy obtained from a battery into ac energy in some oscillatory circuit.

Principle of an oscillator. Fig. 14.87 shows the block diagram of an oscillator. Obviously, an oscillator may be regarded as the self-sustained transistor amplifier with a positive feedback.

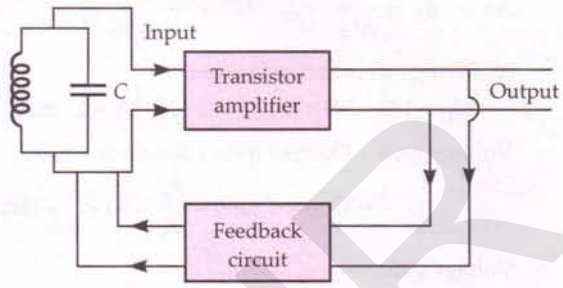


Fig. 14.87 Principle for an oscillator.

Essential parts of a transistor oscillator are :

(*i*) ***Tank circuit.*** A tank circuit is just a parallel combination of an inductance L and a capacitance C. The electric energy once given to it alternately changes between electrostatic energy in the capacitor and the magnetic energy in the inductor. The frequency of electric oscillations in the tank circuit is

$$f = \frac{1}{2\pi\sqrt{LC}}$$

However, the oscillations get damped due to resistive losses in the inductance, and dielectric losses in the capacitor.

(*ii*) ***Transistor amplifier.*** The oscillations of the tank circuit are fed to the transistor amplifier. The oscillations get amplified due to the amplifying action of the transistor.

(*iii*) ***Feedback circuit.*** To compensate for the energy losses occurring in the tank circuit, the feedback circuit returns (feeds back) a part of the output power of the transistor amplifier to the tank circuit *in phase* with the input signal. This process is called *positive feedback* and produces undamped oscillations. The feedback may be done through inductive coupling (mutual inductance).

Transistor as an oscillator. Fig 14.88 shows the basic circuit using a common-emitter *n-p-n* transistor as an oscillator. A tank circuit consisting of an inductance L and a variable capacitor C is connected in the input or

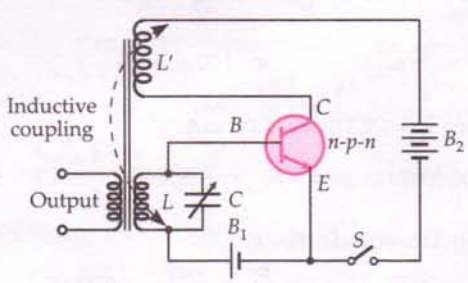


Fig. 14.88

the emitter-base circuit which is forward biased. A small coil L' called *feedback* or *tickler coil* is connected in the output or the emitter-collector circuit which is reverse biased. The coil L' is inductively coupled with the coil L of the tank circuit.

1. **Working.** When the switch S is closed, a small collector current starts growing through coil L'. This increases the magnetic flux linked with coil L' and hence with coil L. This induces *emf* in coil L in the direction of forward bias and a positive charge begins to build on the upper plate of capacitor C. The emitter current increases and also the collector current increases. This increases the magnetic flux linked with L' and hence with L. Consequently, the forward bias increases which further increases the emitter and collector currents. Charging of capacitor continues. This process continues till the collector current becomes maximum.

When the current through L' stops changing, the induced *emf* linked with L vanishes. This decreases the emitter current and hence the collector current. The decreasing current through L' induces *emf* in L in the opposite direction of the forward bias. This results in decrease in the emitter current and hence the collector current. At the same time positive charge on the lower plate of capacitor C begins to build up. The process continues till the collector current becomes zero. (In fact, inertia of the collapsing magnetic field carries the collector current below the zero value). The induced *emf* linked with L again becomes zero, *i.e.*, the forward bias is now not being opposed by induced *emf*. The emitter current and hence the collector current will start increasing. This cycle repeats again and again to give electric oscillations of constant amplitude and of constant frequency,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The oscillations of a desired frequency can be obtained by changing the value of capacitance C of the variable capacitor. In this oscillator, we have connected tank circuit on the base side. Hence, it is known as ***tuned base oscillator.*** If the tank circuit is on the collector side, it will be known as ***tuned-collector oscillator.***

Positive feedback. In common-emitter transistor circuit, a signal applied to the base-emitter circuit appears with a phase change of 180° in the collector-emitter circuit. The coupling of L and L' produces a further phase change of 180° due to mutual induction. Hence the energy fed back to the tank circuit is in phase with the input signal. Due to this positive feedback, the oscillations of the tank circuit are correctly maintained.

For Your Knowledge

➢ **Barkhausen's criterion for sustained oscillations.** When a part of the output is fed back to the input of an amplifier, the process is called *feedback process*. Fig. 14.89 shows a feedback amplifier with input V_s and output V_0. The voltage gain of the feedback amplifier is

$$A'_v = \frac{\text{Output}}{\text{Input}} = \frac{V_0}{V_s}$$

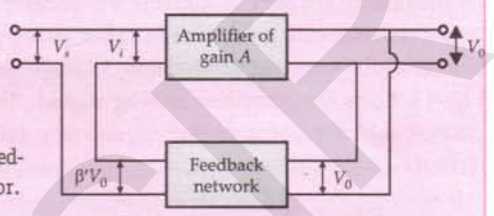


Fig. 14.89 Principle of feed-back oscillator.

➢ The input given to the feedback network is V_0. If β' is the feedback fraction of the feedback network, then output obtained from it is $\beta' V_0$. This fraction is mixed with the signal voltage V_s and is given to the amplifier.

$\therefore$ Input of the amplifier, $V_i = V_s + \beta' V_0$

The voltage gain of the amplifier is

$$A = \frac{\text{Output}}{\text{Input}} = \frac{V_0}{V_s + \beta' V_0}$$

or $AV_s + A\beta' V_0 = V_0$ or $AV_s = V_0 (1 - \beta' A)$

or $$\frac{A}{1 - \beta' A} = \frac{V_0}{V_s}$$

Hence the gain of the feedback amplifier is

$$A'_v = \frac{V_0}{V_s} = \frac{A}{1 - \beta' A}$$

When $\beta' A = 1$, $A'_v = \frac{V_0}{V_s} = \infty$. This means $V_s = 0$.

Thus the output voltage is obtained without the input voltage. The amplifier becomes a self-sustained oscillator. Hence the condition for stable oscillations to be sustained is : $\beta' A = 1$.

This is known as ***Barkhausen criterion*** for sustained oscillations.

➢ If the feedback is negative, the gain of the amplifier becomes $A'_v = \frac{A}{1 + \beta' A}$

➢ In an oscillator, the feedback is in same phase (positive feedback). If the feedback voltage is in opposite phase (negative feedback), the gain is less than 1 and it can never work as an oscillator. It will be an amplifier with reduced gain. However, the negative feedback reduces the noise and distortion of an amplifier.

➢ Different oscillators use different feedback networks (such as inductive coupling or LC or RC networks) for coupling the output to the input apart from the resonant circuit for obtaining oscillations of a particular frequency. These give rise to different types of oscillators like Colpitt's oscillator, Hartley oscillator, RC-oscillator, etc.

14.43 ANALOG AND DIGITAL CIRCUITS

50. *What are analog and digital circuits ? Give examples.*

Analog and digital circuits. All electronic circuits can be broadly divided into *two* categories :

1. Analog circuits.
2. Digital circuits.

1. ***Analog circuits.*** *A signal in which current or voltage varies continuously with time is called* ***analog signal.*** A sinusoidally varying alternating voltage as shown in Fig. 14.90, is the simplest analog signal. *The electronic circuits which process analog signals are called* ***analog circuits.***

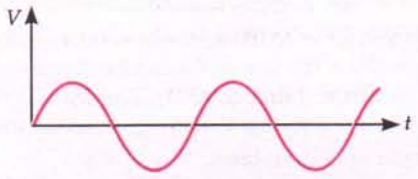


Fig. 14.90 Analog signal.

An *avometer* (ampere-volt-ohm meter) is an analog device. When a current, voltage or a resistance is measured by it, its pointer moves gradually and continuously over a scale. The devices like amplifiers, radio, television, oscillators, etc ; also make use of analog signals.

2. ***Digital circuits.*** *A signal in which current or voltage can take only two discrete values is called a* ***digital signal.*** A digital signal can take only two values 1 and 0 which are labelled as *high* and *low values*. In the square wave-form shown in Fig. 14.91, a signal of 0 V represents binary 0 and a signal of 5 V represents binary 1. Thus digital signals are in the form of pulses of equal level. *The electric circuits which process digital signals are called* ***digital circuits.***

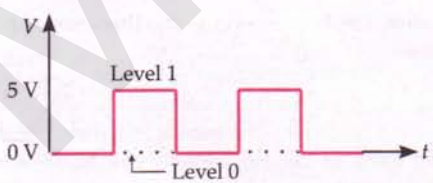


Fig. 14.91 Digital signal or pulse.

A digital multimeter is a digital device. When a current, voltage or a resistance is measured by it, the number displayed by the multimeter increases in small discrete steps. The devices like pocket calculators, electronic watches, video cassette recorders, burglar alarms, robots, modern computers etc. ; are all digital circuits. Digital computers are more fast, reliable and accurate than analog computers.

There are some special circuits which handle the digital data consisting of 0 and 1 levels. This forms the subject of ***Digital Electronics.***

14.44 BOOLEAN ALGEBRA

51. *What is Boolean algebra ?*

Boolean algebra. We come across a number of *two-valued* questions in our daily life such as

1. A statement is true or false.
2. A motive is good or bad.
3. An action is right or wrong.
4. An electric circuit is open or closed.

In such two valued systems, the relation between logic and mathematics was first realised by an English mathematician *George Boole* in 1854. Boole developed an algebra known as *Boolean algebra* for two-valued logical statements. The logical statements are known as *Boolean variables*. A Boolean variable can have either a *true* value or a *false* value. The true value is represented by 1 and false value by 0. For example, the active and passive states of semiconductor devices such as a switch, a diode or a transistor may be represented by 1 and 0, respectively.

In 1938, *Clande Shannon* of Bell telephone laboratories used *Boolean algebra* to design complicated switching circuits. *A switch is a binary device having an* ON *and an* OFF *position.*

14.45 BOOLEAN OPERATORS

52. *Name the three basic operators of Boolean algebra. With the help of simple switch circuits, write their truth tables.*

Boolean Operators. Just as in ordinary algebra, mathematical operators like addition, subtraction and multiplication are used, similarly, in Boolean algebra three basic operators like OR, AND and NOT are used.

The OR operator. As shown in Fig. 14.92, consider a parallel combination of two switches connected in series with a bulb and a battery.

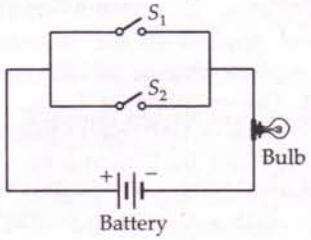


Fig. 14.92 Basic idea of OR operator using simple switches

The bulb will glow when either or both of the switches S_1 and S_2 are closed but it will not glow when both are open. The functioning of the circuit may be summarised in tabular form as follows :

Table 14.1

Switch S_1	Switch S_2	Bulb glows
Open	Open	No
Open	Closed	Yes
Closed	Open	Yes
Closed	Closed	Yes

This action of the switches is called OR operation. Now let S_1 be called input A and S_2 input B. Let the state of the bulb be called output Y. Then the OR operator may be described by the following *Boolean equation or expression* :

$$Y = A + B$$

which is read as 'Y equals A or B'. Now if the ON value of Boolean variable is denoted by 1 and OFF value by 0, then the above table can be rewritten as follows :

Table 14.2 Truth table of OR operator

Input A	Input B	Output $Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

This table is called the truth table of the OR operation. Obviously, the output is 1 when any of the inputs is 1.

The AND operator. As shown in Fig. 14.93, consider two switches S_1 and S_2 connected in series with a bulb and a battery.

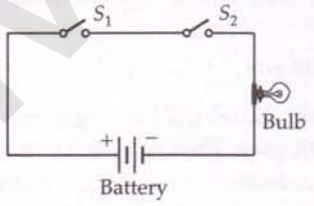


Fig. 14.93 Basic idea of AND operator using simple switches.

The bulb can glow only if both the switches S_1 and S_2 are closed. The operation of the circuit is summarised in the following table :

Table 14.3

Switch S_1	Switch S_2	Bulb glows
Open	Open	No
Open	Closed	No
Closed	Open	No
Closed	Closed	Yes

This action of the switches is called the AND operation. The AND operator relates two input variables A and B to give a new output variable Y and is described by the Boolean expression :

$$Y = A \,.\, B$$

which is read as 'Y equals A and B'. Thus the truth table of AND operator will be as follows :

Table 14.4 Truth table of AND operator

Input A	Input B	Output $Y = A \,.\, B$
0	0	0
0	1	0
1	0	0
1	1	1

Obviously, the output of AND operator is 1 only when both the inputs are 1.

The NOT operator. Consider a bulb short circuited by a switch S, as shown in Fig. 14.94.

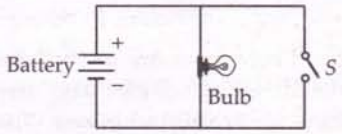


Fig. 14.94 Basic idea of NOT operator using a simple switch.

When the switch S is open, the current flows through the bulb and it glows. When the switch S is closed, the current goes through the switch and the bulb is off (assuming zero resistance of the closed switch). The function of the circuit can be summarised in the following table.

Table 14.5

Switch S	Bulb glows
Open	Yes
Closed	No

This action of the circuit is called NOT operation. Let the switch S be called input A and the state of the bulb be called output Y. Then the NOT operator may be described by the Boolean expression :

$$Y = \overline{A}$$

which is read as 'Y equals not A' or 'Y equals negation A'. Thus the truth table of NOT operator will be as follows :

Table 14.6

Input A	Output $Y = \overline{A}$
0	1
1	0

The NOT operator is an *inverter*. It operates on one Boolean variable and gives its negation or complement as the output. As it operates on only one input variable, so NOT operator is a *unary* operator, unlike OR and AND operators which are binary operators (because they connect two input variables A and B). For example, suppose we define the Boolean variable A as

A = Bhupesh is a student of 12th class

then

$\overline{A}$ (or not A) = Bhupesh is not a student of 12th class

i.e., if $A = 1$ then $\overline{A} = 0$, and vice versa.

14.46 LOGIC GATES

53. *What is a logic gate ? Define truth table and Boolean expression. What are positive and negative logics ?*

Logic gates. Logic gates are the building blocks of digital circuits in which diodes and transistors are used to perform switching functions. They form the heart of digital computers and are widely used in control systems. Basically, a gate is a circuit to provide an output which is dependent on the manner in which the inputs are applied.

A gate is a digital circuit that is designed for performing a particular logical operation. As it works according to some logical relationship between input and output voltages, so it is generally known as a logic gate.

A logic gate may have one or more input terminals but only one output terminal.

There are *three* basic gates :

1. **OR gate**,
2. **AND gate**, and
3. **NOT gate**.

Each logic gate is represented by a graphic symbol and its function is defined either by a truth table or by a Boolean expression.

Truth table. *It is a table that shows all possible input combinations and the corresponding outputs for a logic gate.*

Boolean expression. *It is a shorthand method to describe the functioning of a logic gate in the form of an equation or an expression. It also relates the all possible combinations of the inputs of a logic gate to the corresponding outputs.*

Positive and negative logic. In any digital circuit, the binary numbers 1 and 0 are represented by two voltage levels. If in a system, the higher voltage level represents 1 and the lower voltage level represents 0, then the system is called a *positive logic*. On the other hand, if the higher voltage level represents 0 and the lower voltage level represents 1, then the system is called a *negative logic*.

14.47 THE 'OR' GATE

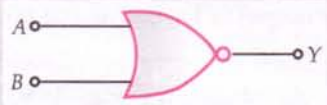
54. *What is an OR gate ? Give Boolean expression, logic symbol and truth table for an OR gate. Explain, with the help of a circuit diagram, how is this gate realised in practice.*

The OR gate. *An OR gate can have any number of inputs but only one output. It gives high output (1) if either input A or B or both are high (1), otherwise the output Y is low (0).*

OR : Output is 1 if input A OR B OR both are 1

Boolean expression : $A + B = Y$

Logic Symbol



Truth Table

Inputs		Output
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 14.95 The OR gate

Figure 14.95 shows the logic symbol and the truth table for an OR gate. The OR gate can be described by the *Boolean expression*

$$A + B = Y$$

which is read as 'A or B equals Y'. Here the plus (+) sign denotes the OR function. It is obvious from the truth table of OR gate that the *output is 1 when any of the inputs is 1.*

Realisation of OR gate. As shown in Fig. 14.96, a two input OR gate can be realised by using two ideal diodes D_1 and D_2 and a resistor R. The negative terminal of the battery is grounded (*i.e.*, it is at zero volt) and corresponds to the 0 state, and the positive terminal (which is at, say 5 V) corresponds to the 1 state.

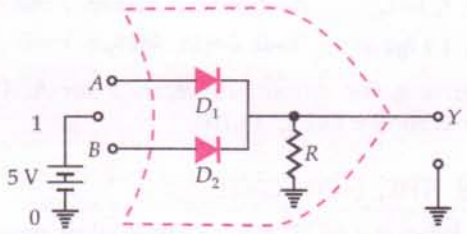


Fig. 14.96 Realisation of OR gate using two *p-n* junction diodes.

The following *four* cases are possible :

1. **When $A = 0$ and $B = 0$.** Both the diodes are connected to earth (0 V). They do not conduct. Output across R is zero, *i.e.*, $Y = 0$.
2. **When $A = 0$ and $B = 1$.** D_1 is connected to earth. It does not conduct. D_2 is connected to 5 V, it gets forward biased and conducts. Voltage drop across D_2 is zero and the full voltage of 5 V appears across R. So $Y = 1$.
3. **When $A = 1$ and $B = 0$.** D_1 gets forward biased and D_2 does not conduct. Voltage drop across R is again 5 V. So $Y = 1$.
4. **When $A = 1$ and $B = 1$.** Both D_1 and D_2 get forward biased and conduct current. But D_1 and D_2 are in parallel. Voltage drop across R is still 5 V. So $Y = 1$.

Hence the circuit shown in Fig. 14.96 satisfies the truth-table of OR gate.

EXAMPLE. *Sketch the output waveform obtained from OR gate for the inputs A and B given in Fig. 14.97.*

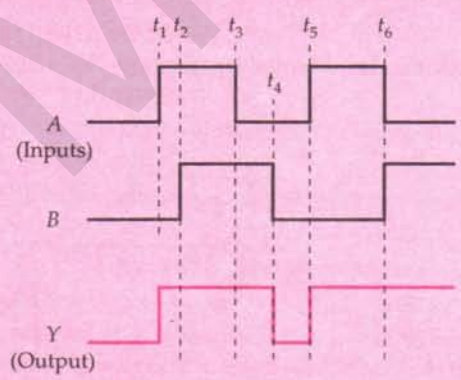


Fig. 14.97 Input and Output waveforms for an OR gate.

Solution. The output of an OR gate is high when either A or B or both the inputs are high. When both the inputs are low, the output is low.

For $t < t_1$;	$A = 0, B = 0$;	Hence $Y = 0$
For t_1 to t_2 ;	$A = 1, B = 0$;	Hence $Y = 1$
For t_2 to t_3 ;	$A = 1, B = 1$;	Hence $Y = 1$
For t_3 to t_4 ;	$A = 0, B = 1$;	Hence $Y = 1$
For t_4 to t_5 ;	$A = 0, B = 0$;	Hence $Y = 0$
For $t > t_6$;	$A = 0, B = 1$;	Hence $Y = 1$

Therefore the output waveform Y will be as shown in Fig. 14.97.

14.48 THE 'AND' GATE

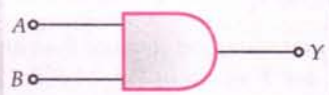
55. *What is an AND gate ? Give Boolean expression, logic symbol and truth table for an AND gate. Explain, with the help of a circuit diagram, how is this gate realised in practice.*

The AND gate. *An AND gate can have any number of inputs but only one output. It gives a high output (1) if inputs A and B are both high (1), otherwise the output Y is low (0).*

AND : Output is 1 if inputs A AND B are 1

Boolean expression : $A . B = Y$

Logic Symbol



Truth Table

Inputs		Output
A	B	$Y = A . B$
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 14.98 The AND gate.

Figure 14.98 shows the logic symbol and the truth table of an AND gate. The AND gate is described by the *Boolean expression* :

$$A . B = Y$$

which is read as 'A and B equals Y'. Here the dot (.) sign represents the AND function. It is obvious from the truth table of AND gate that the *output is 1 only when both the inputs are 1.*

Realisation of AND gate. As shown in Fig. 14.99, a two input AND gate can be realised by using two ideal junction diodes D_1 and D_2. Here the resistance R is kept permanently connected to the +ve terminal of 5 V battery.

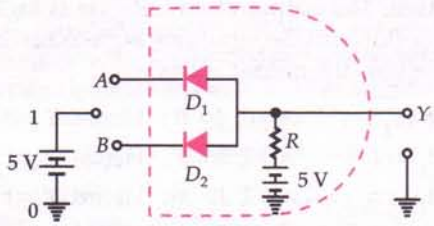


Fig. 14.99 Realisation of an AND gate.

The following *four* cases are possible :

1. **When $A = 0$ and $B = 0$.** The input terminals A and B are earthed (0 V). The two diodes get forward biased and conduct current. But both diodes are shorted. The point Y also gets earthed through the shorted diodes. Hence output $Y = 0$.
2. **When $A = 0$ and $B = 1$.** Diode D_1 is forward biased but shorted. Diode D_2 is not forward biased and does not conduct. Hence output $Y = 0$.
3. **When $A = 1$ and $B = 0$.** D_1 does not conduct. D_2 is forward biased but shorted. Hence output $Y = 0$.
4. **When $A = 1$ and $B = 1$.** Both D_1 and D_2 do not conduct as they are not forward biased. The output voltage is equal to the battery voltage of 5 V. Hence $Y = 1$.

Hence the circuit shown in Fig. 14.99 satisfies the truth table of AND gate.

EXAMPLE. *Sketch the output waveform obtained from an AND gate for the inputs A and B shown in Fig.* 14.100.

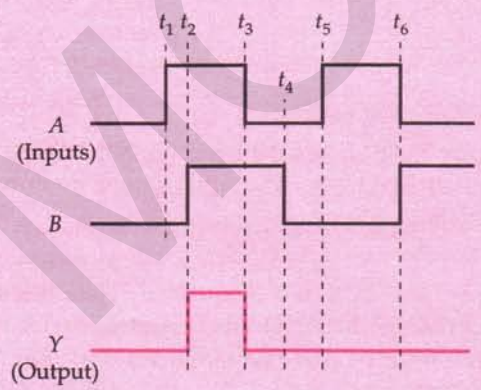


Fig. 14.100 Input and output wavefroms for an AND gate.

Solution. The output of an AND gate is high when both the inputs are high, otherwise the output is low.

For $t \le t_1$;	$A = 0, B = 0$;	Hence $Y = 0$
For t_1 to t_2 ;	$A = 1, B = 0$;	Hence $Y = 0$
For t_2 to t_3 ;	$A = 1, B = 1$;	Hence $Y = 1$
For t_3 to t_4 ;	$A = 0, B = 1$;	Hence $Y = 0$
For t_4 to t_5 ;	$A = 0, B = 0$;	Hence Y
For t_5 to t_6 ;	$A = 1, B = 0$;	Hence $Y = 0$
For $t > t_6$;	$A = 0, B = 1$;	Hence $Y = 0$

Therefore, the output waveform Y for AND gate will be as shown in Fig. 14.100.

14.49 THE 'NOT' GATE

56. *What is a NOT gate ? Give Boolean expression, logic symbol and truth table for a NOT gate. Explain, with the help of a circuit diagram, how is this gate realised in practice.*

The NOT gate. *A NOT gate is the simplest gate, with one input and one output. It gives a high output (1), if the input A is low (0), and vice versa. Whatever the input, the NOT gate inverts it.*

Figure 14.101 shows the logic symbol and the truth table of NOT gate. The NOT gate is described by the *Boolean expression* :

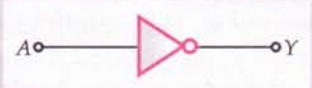
$$\overline{A} = Y$$

which is read as 'not A equals Y', *i.e.*, Y is the negation A. This means that $Y = 0$ if $A = 1$ and $Y = 1$ if $A = 0$.

NOT : Output is high if input is low, NOT high and vice versa

Boolean expression : $\overline{A} = Y$

Logic Symbol



Truth Table

Input	Output
A	Y
0	1
1	0

Fig. 14.101 The NOT gate.

Realisation of NOT gate. As shown in Fig. 14.102, a NOT gate can be obtained by using an *n-p-n* transistor.

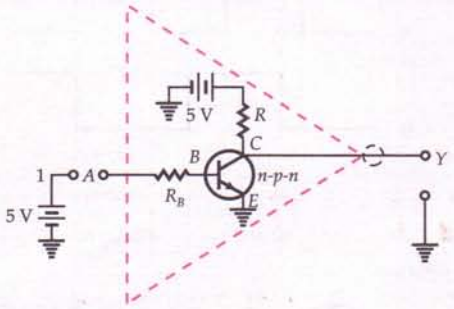


Fig. 14.102 Realisation of a NOT gate using a transistor.

The base resistor R_B and the collector resistance R_C are so chosen that when a voltage of 5 V is applied at the base of the transistor, a large collector current flows, the voltage at Y drops and the base-collector junction is forward biased.

The following *two* cases are possible :

1. **When input $A = 0$.** The base of the transistor is earthed, the base-emitter junction is not forward biased and the collector-base junction is reverse biased. Hence the base current and the collector current are both zero. The transistor is in the *cut-off* mode. No voltage drop occurs across R_C. The voltage at Y is 5 V. Hence output $Y = 1$.
2. **When input $A = 1$.** The input terminal A is at 5 V, both emitter and collector are forward biased. A large collector current flows. The transistor is in the *saturation mode*. The voltage drop across R_C is almost 5 V. Hence output $Y = 0$.

Thus, the circuit of Fig. 14.102 satisfies the truth table of a NOT gate.

EXAMPLE. *Sketch the output waveform obtained from a NOT gate for the input A shown in Fig.* 14.103.

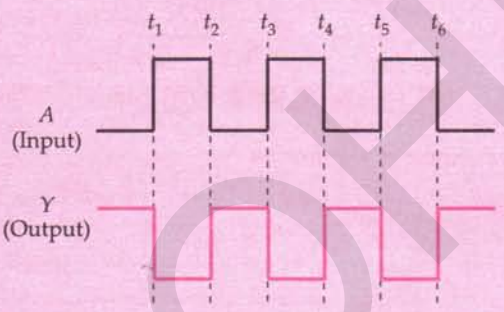


Fig. 14.103 Input and output waveforms for a NOT gate.

Solution. The output of a NOT gate is high when the input is low and vice versa.

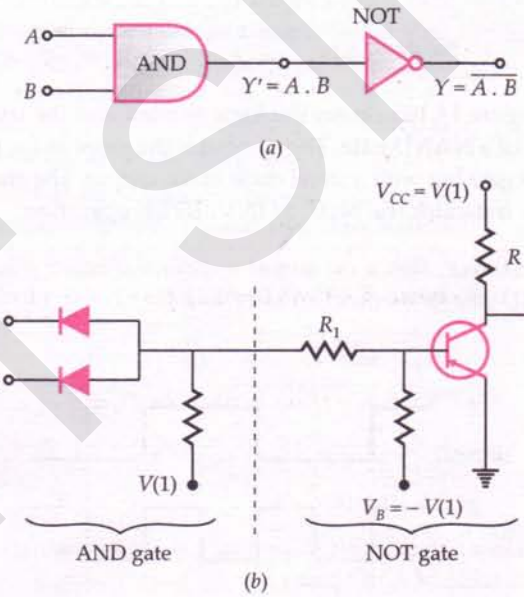
For $t \le t_1$;	$A = 0$;	Hence $Y = 1$
For t_1 to t_2 ;	$A = 1$;	Hence $Y = 0$
For t_2 to t_3 ;	$A = 0$;	Hence $Y = 1$
For t_3 to t_4 ;	$A = 1$;	Hence $Y = 0$
For t_4 to t_5 ;	$A = 0$;	Hence $Y = 1$
For t_5 to t_6 ;	$A = 1$;	Hence $Y = 0$
For $t > t_6$;	$A = 0$;	Hence $Y = 1$

Therefore, the output waveform Y from NOT gate is as shown in Fig. 14.103.

14.50 THE 'NAND' GATE

57. *What is a NAND gate ? How is it realised in practice ? Give the logic symbol, Boolean expression and truth table for a NAND gate.*

The NAND (NOT AND) gate. A NAND gate is a combination of an AND and a NOT gate. It is obtained by connecting the output of an AND gate to the input of a NOT gate, as shown in Fig. 14.104. Its truth table can be obtained by using the truth table of AND gate and then finding the negation of its output.



A	B	$Y' = A.B$	$Y = \overline{A.B} = \overline{Y'}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

(c)

Fig. 14.104 Realisation of a NAND gate (*a*) Logic circuit (*b*) Practical circuit diagram (*c*) Logic table.

The NAND gate is described by the *Boolean expression* :

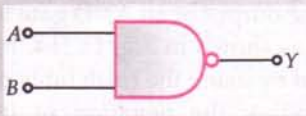
$$\overline{A \,.\, B} = Y \quad \text{or} \quad \overline{AB} = Y$$

which is read as 'A AND B negated equals Y'. *The output of a NAND gate is low when both the inputs are high otherwise high.*

NAND : Output is 1 if input A AND input B are NOT both 1

Boolean expression : $\overline{A.B} = Y$

Logic Symbol



Truth Table

Inputs		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 14.105 The NAND gate.

Figure 14.105 shows the logic symbol and the truth table of a NAND gate. The symbol is the same as for the AND gate but with a small circle at the output. The small circle indicates the NOT or INVERTER operation.

EXAMPLE. *Sketch the output waveform obtained from a NAND gate for the inputs A and B as shown in Fig. 14.106.*

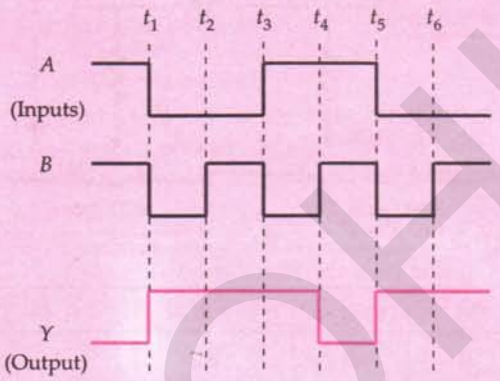


Fig. 14.106 Input and output waveforms from NAND gate.

Solution. The output of a NAND gate is low when both the inputs are high otherwise it is high.

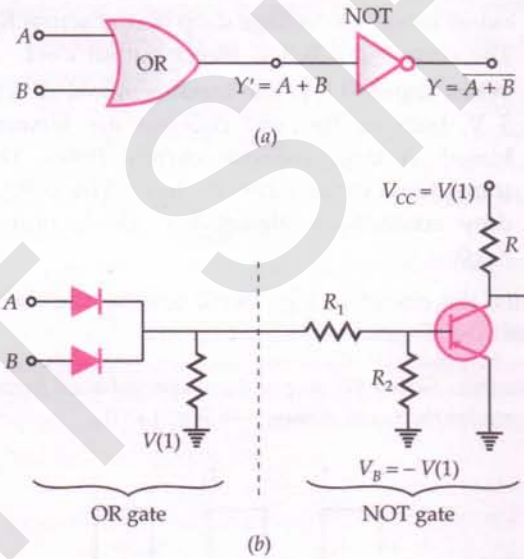
For $t < t_1$; $A = 1, B = 1$; Hence $Y = 0$
For t_1 to t_2 ; $A = 0, B = 0$; Hence $Y = 1$
For t_2 to t_3 ; $A = 0, B = 1$; Hence $Y = 1$
For t_3 to t_4 ; $A = 1, B = 0$; Hence $Y = 1$
For t_4 to t_5 ; $A = 1, B = 1$; Hence $Y = 0$
For t_5 to t_6 ; $A = 0, B = 0$; Hence $Y = 1$
For $t > t_6$; $A = 0, B = 1$; Hence $Y = 1$

Therefore, the output waveform for NAND gate will be as shown in Fig. 14.106.

14.51 THE 'NOR' GATE

58. *What is a NOR gate ? How is it realised in practice ? Give the logic symbol, Boolean expression and truth table for a NOR gate.*

The NOR (NOT OR) gate. A NOR gate is a combination of an OR and a NOT gate. It is obtained by connecting the output of an OR gate to the input of a NOT gate, as shown in Fig. 14.107. Its truth table can be obtained by using the truth table of an OR gate and then finding the negation of its output.



A	B	$Y' = A + B$	$Y = \overline{A + B} = \overline{Y'}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(c)

Fig. 14.107 Realisation of a NOR gate (*a*) Logic circuit (*b*) Practical circuit diagram (*c*) Logic table.

The NOR gate is described by the *Boolean expression* :

$$Y = \overline{A + B}$$

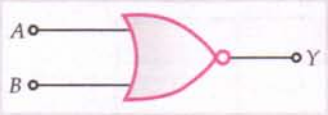
which is read as 'A OR B negated equals Y'. *The output of a NOR gate is high when both the inputs are low otherwise low.*

Figure 14.108 shows the logic symbol and the truth table of a NOR gate.

NOR : Output is 1 if neither input A NOR input B is 1

Boolean expression : $\overline{A+B}=Y$

Logic Symbol



Truth Table

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 14.108 The NOR gate.

EXAMPLE. *Sketch the output waveform obtained from a NOR gate for the inputs A and B shown in Fig. 14.109.*

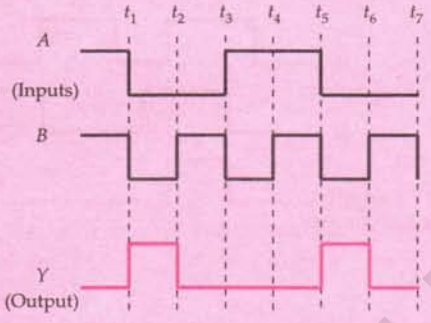


Fig. 14.109 Input and output waveforms from NOR gate.

Solution. The output of a NOR gate is high when both the inputs are low otherwise it is low.

For $t<t_1$;	$A=1, B=1$;	Hence $Y=0$
For t_1 to t_2 ;	$A=0, B=0$;	Hence $Y=1$
For t_2 to t_3 ;	$A=0, B=1$;	Hence $Y=0$
For t_3 to t_4 ;	$A=1, B=0$;	Hence $Y=0$
For t_4 to t_5 ;	$A=1, B=1$;	Hence $Y=0$
For t_5 to t_6 ;	$A=0, B=0$;	Hence $Y=1$
For t_6 to t_7 ;	$A=0, B=1$;	Hence $Y=0$

14.52 NAND AND NOR GATES AS DIGITAL BUILDING BLOCKS

59. *Why are NAND and NOR gates also called universal gates ?*

NAND and NOR gates as digital building blocks. The repeated use of the OR, the AND or the NOT gates alone cannot give a different gate. But the repeated use of the NAND or the NOR gates alone can give all basic gates like OR, AND and NOT gates. Hence the NAND and the NOR gates are also called ***universal gates***. In digital circuits, these gates serve as digital building blocks. Refer to Examples 48 and 49 on page 14.59 and Examples 51 and 52 on page 14.60.

Examples based on Logic Gates

Concepts Used

1. **OR gate.** It gives high output when either of the inputs is high, otherwise it gives low output.
$$Y = A + B$$
2. **AND gate.** It gives high output when both the inputs are high, otherwise the input is low.
$$Y = A \,.\, B$$
3. **NOT gate.** It gives high output when the input is low, and vice versa.
$$Y = \overline{A}.$$
4. **NAND gate.** It gives low output when both the inputs are high, otherwise the output is high.
$$Y = \overline{A \,.\, B}$$
5. **NOR gate.** It gives high output when both the inputs are low, otherwise the output is low.
$$Y = \overline{A + B}.$$

Example 43. *Justify the output waveform (Y) of the OR gate for inputs (A) and (B) as given in Fig. 14.110.* [CBSE D 05]

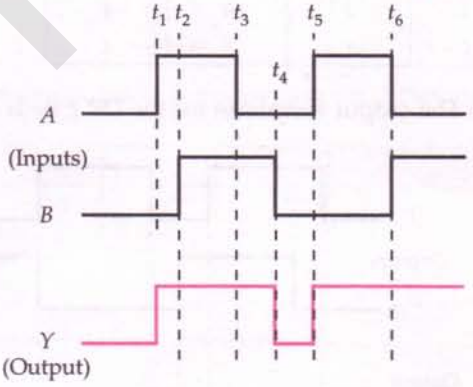


Fig. 14.110

Solution. From the given waveforms, we note that

Time interval	Input A	Input B	Output Y
$t<t_1$	0	0	0
$t_1<t<t_2$	1	0	1
$t_2<t<t_3$	1	1	1
$t_3<t<t_4$	0	1	1
$t_4<t<t_5$	0	0	0
$t_5<t<t_6$	1	0	1
$t<t_6$	0	1	1

Clearly, the output $Y = A + B$. Hence the output waveform (Y) of the OR gate for the inputs (A) and (B) is justified.

Example 44. *In Fig. 14.111 below, circuit symbol of a logic gate and two input waveforms 'A' and 'B' are shown.*

(a) Name the logic gate. (b) Write its truth table.

(c) Give the output waveform. [CBSE D 02C, OD 04]

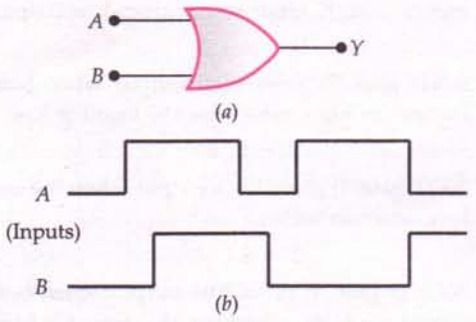


Fig. 14.111

Solution. (*a*) The given logic gate is an OR gate.

(*b*) Truth table of OR gate

Input *A*	Input *B*	Output *Y*
0	0	0
0	1	1
1	0	1
1	1	1

(*c*) The output waveform for the OR gate is shown below.

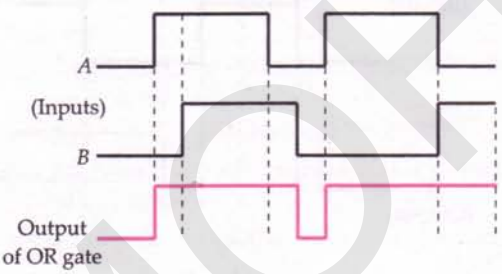


Fig. 14.112

Example 45. *In Fig. 14.113 below, circuit symbol of a logic gate and two input waveforms 'A' and 'B' are shown.*

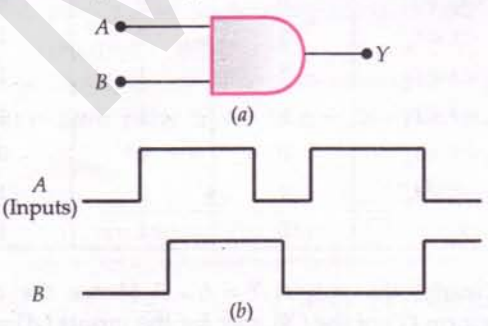


Fig. 14.113

(a) Name the logic gate.

(b) Write its truth table.

(c) Give the output waveform. [CBSE D 02C, OD 04]

Solution. (*a*) The given logic gate is an AND gate.

(*b*) Truth table of AND gate

Input *A*	Input *B*	Output *Y*
0	0	0
0	1	0
1	0	0
1	1	1

(*c*) The output waveform for the AND gate is shown below.

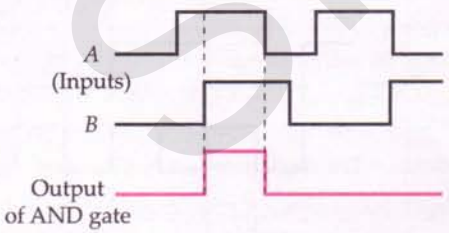


Fig. 14.114

Example 46. *In the figure below, circuit of a logic gate and input waveform is shown. (i) Name the logic gate, (ii) write its truth table and (iii) give the output waveform.* [CBSE D 03]

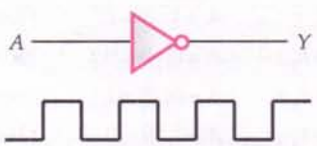


Fig. 14.115

Solution. (*i*) The logic gate is a NOT gate.

(*ii*) Truth table of NOT gate

Input *A*	Output $Y = \bar{A}$
0	1
1	0

(*iii*) The output waveform for the NOT gate is given below.

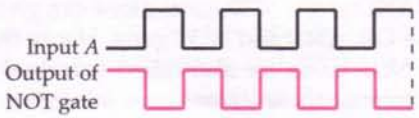


Fig. 14.116

Example 47. *In the figure below, circuit symbol of a logic gate and two input waveforms 'A' and 'B' are shown.*

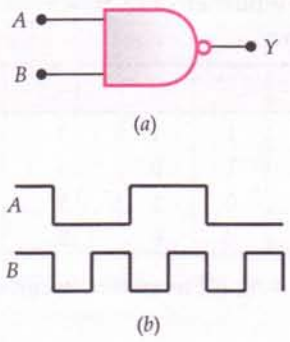


Fig. 14.117

(*i*) *Name the logic gate.*
(*ii*) *Write its truth table.*
(*iii*) *Give the output waveform.*

[CBSE D 02C]

Solution. (*i*) The logic gate is a NAND gate.

(*ii*) Truth table of NAND gate is

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

(*iii*) The output waveform for the NAND gate is shown below.

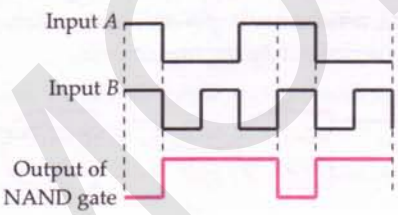


Fig. 14.118

Example 48. *Write the truth table for circuit given in Fig. 14.119 below consisting of NOR gates and identify the logic operation (OR, AND, NOT) which this circuit is performing.* [NCERT]

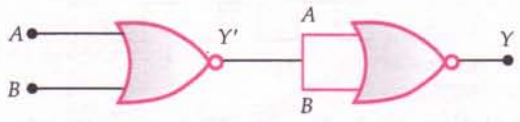


Fig. 14.119

Solution. The first gate is a NOR gate. The second gate is also a NOR gate with both the input terminals connected together.

The logic table for the above circuit is as follows :

First NOR gate				Second NOR gate		
A	B	$A+B$	$Y'=\overline{A+B}$	$A=Y'$	$B=Y'$	$Y=\overline{A+B}$
0	0	0	1	1	1	0
0	1	1	0	0	0	1
1	0	1	0	0	0	1
1	1	1	0	0	0	1

Clearly, $Y = \overline{A+B} = A + B$.

Thus the given circuit performs OR operation.

Example 49. *Write the truth table for circuit given in Fig. 14.120 consisting of NOR gates only. Identify the logic operations (OR, AND, NOT) performed by the two circuits.*

[NCERT ; CBSED 09C, 15C, OD 11]

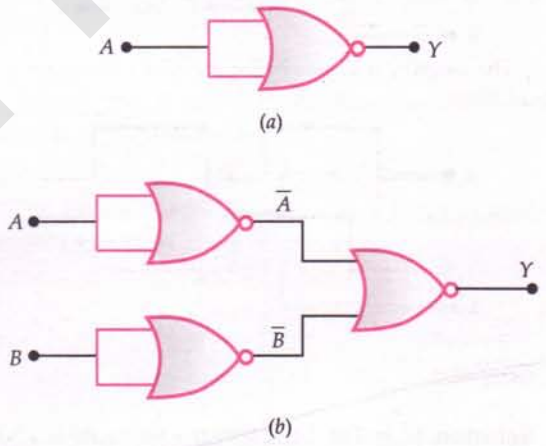


Fig. 14.120

Solution. (*i*) The circuit of Fig. 14.120(*a*) is a NOR gate with both its input terminals connected together. The output of a NOR gate is high when both its inputs are low. Keeping this in mind, we can write the truth table as follows :

A	$B=A$	$Y=\overline{A+B}$
0	0	1
1	1	0

Clearly, $Y = \overline{\overline{A} + \overline{B}} = \overline{A}$.

Hence a NOR gate with both its input terminals connected together performs the NOT operation.

(*ii*) Here the inputs A and B get inverted by the two NOT gates (made from NOR gates). The outputs $\overline{A}$ and $\overline{B}$ are fed to a NOR gate. The output of a NOR gate is high when both the inputs are low. So we write the truth table as follows :

A	B	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$	$Y = \overline{\overline{A} + \overline{B}}$
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

Clearly $Y = \overline{\overline{A} + \overline{B}} = A \,.\, B$. Hence the circuit of Fig. 14.120(*b*) performs the function of an AND gate.

Example 50. *You are given the two circuits as shown in Fig. 14.121. Show that the circuit (a) acts as OR gate while the circuit (b) acts as AND gate.* [NCERT]

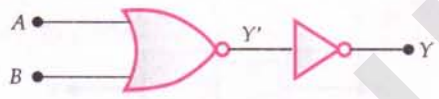
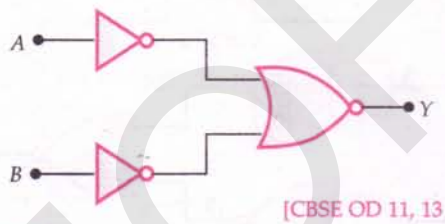


Fig. 14.121(*a*)



[CBSE OD 11, 13 ; D 14C]

Fig. 14.121(*b*)

Solution. (*i*) In Fig. 14.121(*a*), the first gate is a NOR gate which gives high output when both its inputs are low. Its output is then fed to a NOT gate. So we can write the truth table as follows :

A	B	$A + B$	$Y' = \overline{A + B}$	$Y = \overline{Y'}$
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	0	1

Clearly, $Y = A + B$. Hence this circuit acts as an OR gate.

(*ii*) In Fig. 14.121(*b*), the outputs of two NOT gates are fed to a NOR gate. The NOR gate gives high output when both its inputs are low. So we can write the truth table as follows :

A	B	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$	$Y = \overline{\overline{A} + \overline{B}}$
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

Clearly, $Y = A \,.\, B$. Hence this circuit acts as an AND gate.

Example 51. *Write the truth table for a NAND gate connected as given in Fig. 14.122. Hence identify the exact logic operation carried out by this circuit.* [NCERT]

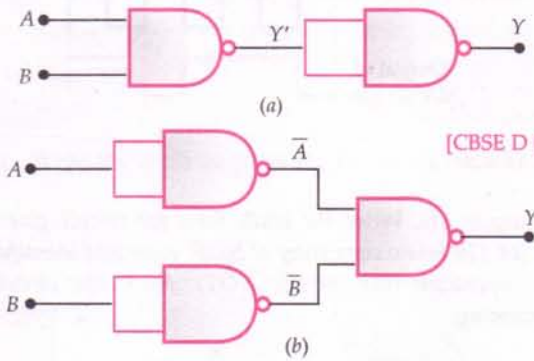
Fig. 14.122

Solution. Here both the input terminals of a NAND gate are connected together. The output of a NAND gate is low when both the inputs are high. So we can write the truth table for the given circuit as follows :

A	$B = A$	$A \,.\, B$	$Y = \overline{A \,.\, B}$
0	0	0	1
1	1	1	0

Clearly, output $Y = \overline{A}$. *Hence a NAND gate with both its input terminals connected together acts as a NOT gate.*

Example 52. *You are given two circuits as shown in Fig. 14.123, which consist of NAND gates. Identify the logic operation carried out by the two circuits.* [NCERT]



[CBSE D 09C]

[CBSE OD 11, 13, D 11]

Fig. 14.123

Solution. (*i*) In Fig. 14.123(*a*), the first gate is a NAND gate. Its output is fed to a NOT gate (made

from a NAND gate). The output of a NAND gate is low when both the inputs are high. So we can write the truth table as follows :

A	B	$A.B$	$Y' = \overline{A.B}$	$Y = \overline{Y'}$
0	0	0	1	0
0	1	0	1	0
1	0	0	1	0
1	1	1	0	1

Clearly, output $Y = A + B$. Hence the given circuit performs the function of an AND gate.

(*ii*) In Fig. 14.123(*b*), the inputs of two NOT gates (made from NAND gates) are fed to a NAND gate. The output of a NAND gate is low when both the inputs are high. So we can write the truth table as follows :

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$	$Y = \overline{\overline{A}.\overline{B}}$
0	0	1	1	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	0	0	1

Clearly, output $Y = A + B$. Hence the given circuit performs the function of an OR gate.

Example 53. *(i) Identify the logic gates marked P and Q in the given logic circuit.*

(ii) Write down the output at Y for the inputs $A = 0, B = 0$ and $A = 1, B = 1$. [CBSE OD 10]

Fig. 14.124

Solution. P is a NOT gate and Q is an OR gate. The input A gets inverted before it reaches the OR gate. Thus the upper input to the OR gate is $\overline{A}$. The final output is

$$Y = \overline{A} + B$$

This is the Boolean equation for the given circuit. The truth table is as follows :

A	B	$\overline{A}$	$Y = \overline{A} + B$
0	0	1	1
0	1	1	1
1	0	0	0
1	1	0	1

For $A = 0$ and $B = 0$, $Y = 1$

For $A = 1$ and $B = 1$, $Y = 1$

Example 54. *Express by a truth table the output Y for all possible inputs A and B in the circuit shown in Fig. 14.125.* [NCERT ; CBSE D 14]

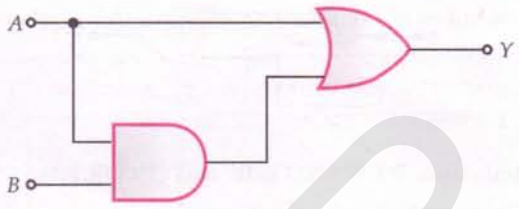


Fig. 14.125

Solution. The given circuit includes an AND and an OR gate, as shown in Fig. 14.126.

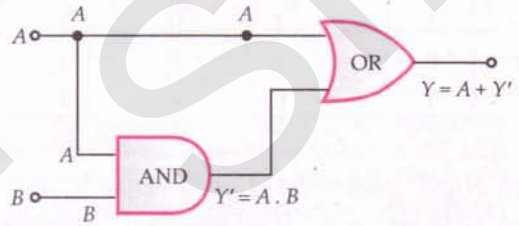


Fig. 14.126

Inputs A and B are fed to AND gate so that its output is

$$Y' = A.B$$

Then inputs A and Y' $(= A.B)$ are fed to OR gate so that the output from it is

$$Y = A + A.B$$

The logic table for the given circuit is as follows :

AND gate			OR gate		
Inputs		Output	Inputs		Output
A	B	$Y' = A.B$	A	Y'	$Y = A + Y'$
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	1	0	1
1	1	1	1	1	1

Hence the truth table is

Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

Example 55. *Identify the logic gates marked 'P' and 'Q' in the given circuit. Write the truth table for the combination.* [CBSE D 14]

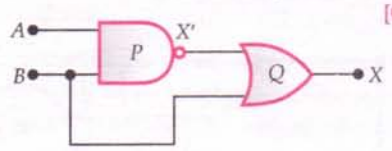


Fig. 14.127

Solution. P = NAND gate and Q = OR gate.

Truth table for the combination :

Inputs		Output of gate P $X' = \overline{A.B}$	Output of gate Q $X = B + X'$
A	B		
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	1

Example 56. *A student has to use an appropriate number of*

(i) NAND gates (only) to get the output Y_1, and

(ii) NOR gates (only) to get the output Y_2, from the two given inputs A and B as shown in Fig. 14.128.

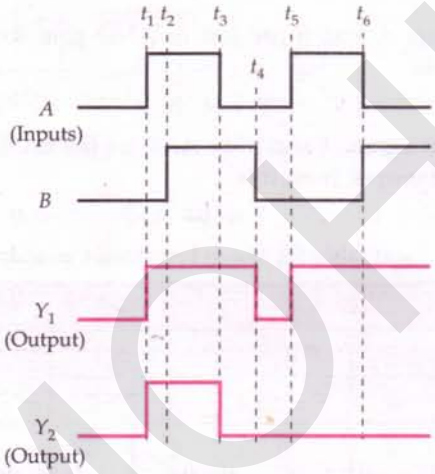


Fig. 14.128

Identify the 'equivalent gate' needed in each case. Show how one can connect an appropriate number of (i) NAND (ii) NOR gates respectively in the two cases to get these 'equivalent gates'. [CBSE SP 15]

Solution. Clearly, the equivalent gate for output Y_1 is an *OR* gate and that for output Y_2 is an AND gate.

(*i*) A combination of three NAND gates, when connected together in the manner shown in Fig. 14.123(*b*), is equivalent to an *OR* gate.

(*ii*) A combination of three NOR gates, when connected together in the manner shown in Fig. 14.120(*b*), is equivalent to an AND gate.

Problems For Practice

1. Write the truth table for the combination of the gates shown. Name the gates used. **[CBSE D 14]**

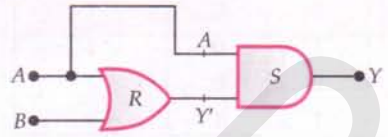


Fig. 14.129

2. Identify the logic gates marked X, Y in the following figure. Write down the output Z, when $A = 1$, $B = 1$ and $A = 0$, $B = 0$.

Fig. 14.130

3. For the given combination of gates, find the values of outputs Y_1 and Y_2 in the table given below. Identify the gates G_1 and G_2.

A	B	C	D
0	0	0	Y_1
1	1	0	Y_2

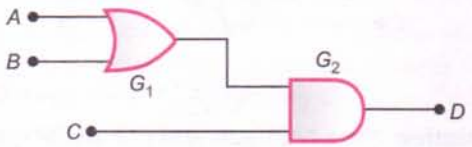


Fig. 14.131

[CBSE Sample Paper 11]

4. Write the truth table for the following circuit :

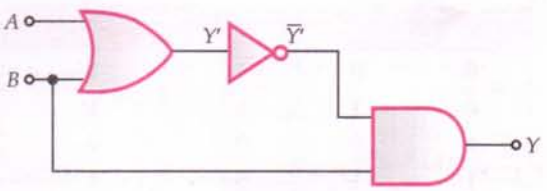


Fig. 14.132

5. Write the logic table for the following circuit :

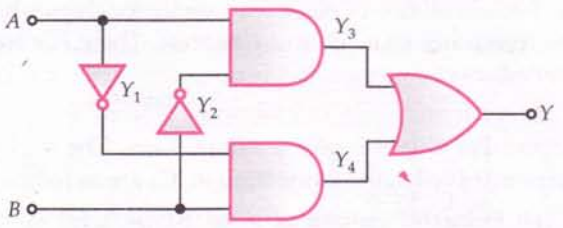


Fig. 14.133

6. Write the truth table for the following circuit. Give the name of the resulting gate. [AIEEE 12]

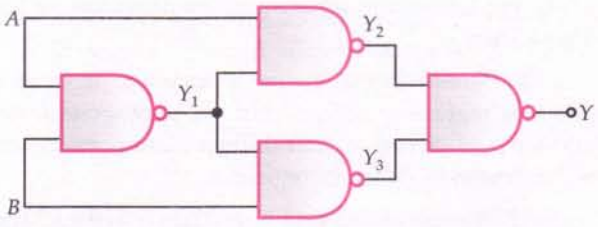


Fig. 14.134

7. Find the output Y of the following circuit if the inputs are : $A = 0, B = 0$; $A = 0, B = 1$, $A = 1, B = 0$; $A = 1, B = 1$.

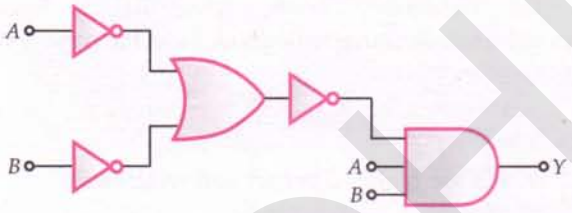


Fig. 14.135

HINTS

1. R = OR gate and S = AND gate.

Inputs		Output of gate R $Y' = A + B$	Output of gate S $Y = A.Y'$
A	B		
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

2. X is OR gate and Y is NOT gate.

Input A	Input B	Output of OR gate $Y = A + B$	Output of NOT gate $Z = \bar{Y}$
1	1	1	0
0	0	0	1

3. G_1 = OR gate, G_2 = AND gate

$Y_1 = 0$ and $Y_2 = 0$

4. When all the inputs are high, the output is 1.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

5.

A	B	Y_1	Y_2	Y_3	Y_4	Y
0	0	1	1	0	0	1
0	1	1	0	0	1	0
1	0	0	1	1	0	0
1	1	0	0	0	0	1

6.

A	B	Y_1	Y_2	Y_3	Y
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

The resulting gate is an exclusive OR (XOR) gate.

7.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

14.53 INTEGRATED CIRCUITS*

60. *What are integrated circuits ? How are they classified ? State the various steps involved in the fabrication of an integrated circuit. Give some advantages and disadvantages of ICs over conventional discrete circuits.*

Integrated circuits. The conventional circuit formed by connecting resistors, inductors, capacitors, diodes, transistors, etc. together, is called a *discrete circuit*. The discrete circuits are (*i*) bulky, (*ii*) less reliable and (*iii*) less shockproof. In their persuit of the miniaturisation of electronic circuits, the electronic engineers started a new branch of electronics, called *microelectronics* in early 1960s. This branch deals with microelectronic circuits, called integrated circuits, abbreviated as ICs.

A miniature electronic circuit, consisting of many passive components like R and C and active devices like diode and transistor, fabricated within a single semiconductor chip is called an integrated circuit.

The first integrated chip was developed in 1958 by *J.S. Kilby* at Texas instruments. Such circuits have revolutionised the electronics technology.

Classification of integrated circuits. The integrated circuits can be classified on the basis of their applications and the methods of their fabrication.

A. ***On the basis of the applications,*** ICs are further classified as follows :

1. *Linear ICs.* These are used for analog functions.
2. *Non-linear ICs.* These are used for digital or switching functions.

B. ***On the basis of the method of fabrication,*** ICs are classified as follows :

1. *Monolithic ICs.* The most widely used technology is the *monolithic integrated circuit*. The word monolithic is derived from two Greek words : *monos* means single and *lithos* means stone. This means that the entire circuit is formed on a single silicon crystal (or chip) as small as 1 mm × 1 mm or even smaller than this size.

On the basis of the number of circuit components or logic gates, the monolithic ICs are further classified as follows :

(*i*) ***Small Scale Integration (SSI) circuits.*** Here the number of logic gates $N \leq 10$.

Examples of SSI chips are 7400, 7320, etc.

(*ii*) ***Medium Scale Integration (MSI) circuits.*** Here $10 < N \leq 100$.

Examples are adders, counters, decoders, etc.

(*iii*) ***Large Scale Integration (LSI) circuits.*** Here $100 < N \leq 100{,}000$.

Examples are Read/Write (R/W), Memory, Read Only Memory (ROM), Shift registers, etc.

(*iv*) ***Very Large Scale Integration (VLSI) circuits.*** Here $100{,}000 < N \leq 10^6$.

Examples are micro-processor chips.

(*v*) ***Ultra Large Scale Integration (ULSI) circuits.*** Here $N > 10^6$.

2. *Film ICs.* In these ICs, the components like resistors, capacitors and thin film transistors are formed on an insulating substrate.

3. *Hybrid ICs.* These ICs consist of combinations of two or more integrated circuits or one integrated circuit and some discrete elements.

4. *Multichip ICs.* In multiple chip, the components are formed on two or more semiconductor chips which are separately attached to a substrate. These ICs have limited use.

Steps involved in the fabrication of an integrated circuit. For this we take a *silicon wafer*. The various steps involved in the fabrication of ICs are as follows :

(*i*) ***Epitaxial growth*** of *n*- or *p*-type layer on the silicon chip, whenever desired. The process involves cracking of silane.

(*ii*) ***Oxidation*** forms an insulating layer of SiO_2 which can be used to separate different regions of the silicon chip.

(*iii*) ***Photolithography*** is a process in which different regions of silicon chip are photographically selected and etched so that different components can be fabricated in different regions.

(*iv*) ***Diffusion*** of different impurities into the silicon chip to form structures of different devices.

(*v*) ***Metallisation*** is the process of deposition of metal films which inter-connect different components on a chip so as to obtain a circuit.

The technology of IC fabrication is highly complicated. But large scale production have made ICs very inexpensive.

Advantages of ICs over conventional discrete circuits :

1. ICs are highly compact and weightless.
2. They have high reliability.
3. They are shock-proof.
4. They have lower total cost.
5. They require low power for their operation.
6. They offer improved performance even at high temperatures.

Drawbacks of ICs :

(*i*) If any one component of an IC gets out of order, the entire IC has to be replaced.

(*ii*) Inductors, transformers and large capacitances cannot be formed on an IC.

(*iii*) It is not possible to fabricate high power (>10 watts) integrated circuits.

Uses of ICs. The integrated circuits are widely used in televisions, microcomputers, radio, video cassette records, pocket calculators and electronic watches. The availability of highly advanced configurations of computers in the market has been made possible by IC technology.

VERY SHORT ANSWER CONCEPTUAL PROBLEMS

Problem 1. Where does the Fermi level lie in a conductor, insulator and semiconductor ?

Solution. The fermi level in conductors lies in the conduction band, in insulators it lies in the valence band and in semiconductors, it lies in the gap between the conduction band and the valence band.

Problem 2. Where does the fermi-level of an intrinsic semiconductor lie ?

Solution. As shown in Fig. 14.136, the fermi level of an intrinsic semiconductor lies midway between its valence and conduction bands. It is just an abstraction. Just as the centre of gravity of a hollow body lies at a point where there is no matter, so also the Fermi level lies in the region of forbidden energy.

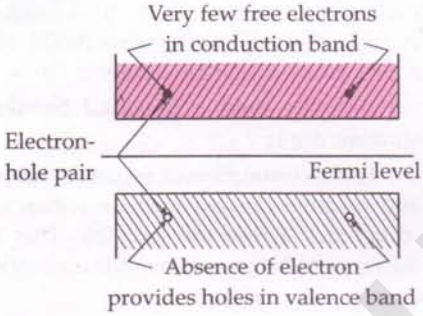


Fig. 14.136

Problem 3. Why does diamond behave like an insulator ?

Solution. There is a large forbidden band of 6 eV in diamond. It is difficult to excite the electrons from valence band to the conduction band. Due to the absence of free charge carriers, diamond behaves as an insulator.

Problem 4. Name two factors on which electrical conductivity of a pure semiconductor at a given temperature depends. [CBSE OD 05C]

Solution. (*i*) The width of the forbidden band (*ii*) Intrinsic charge carrier concentration.

Problem 5. How does the conductivity of a semiconductor change with the rise in its temperature ? [CBSE OD 95C ; D 95C]

Solution. The conductivity of a semiconductor increases exponentially with temperature.

Problem 6. Why does the conductivity of a semiconductor increase with rise of temperature ? [Haryana 93 ; CBSE Sample Paper 97]

Solution. When a semiconductor is heated, more and more electrons jump across the forbidden gap from valence band to conduction band where these are free to conduct electricity. Hence the conductivity increases with the increase in temperature.

Problem 7. Why does a semiconductor get damaged when a heavy current flows through it ? [Himachal 10 ; Punjab 04 ; CBSE F 94]

Solution. When a heavy current flows, the semiconductor gets heated up. Many covalent bonds break liberating a large number of free electrons. The semiconductor loses its property of controlled conduction. It becomes an ordinary conductor.

Problem 8. Why it is difficult to make intrinsic semiconductors ?

Solution. An intrinsic semiconductor has to be extremely pure with a purity level of 99.9999%. It is very difficult to get this much purity.

Problem 9. The conductivity of an intrinsic semiconductor is very low. Why ?

Solution. An intrinsic semiconductor has a very small concentration of free electrons and holes ($\approx 10^{16}\,m^{-3}$) so it has a low conductivity.

Problem 10. The forbidden energy band of silicon is 1.1 eV. What does it mean ?

Solution. This means that if an energy of 1.1 eV is given to an electron in the valence band, it will jump to the conduction band.

Problem 11. What is doping in semiconductor ? Why is it done ? [ISCE 95, 97, 01]

Solution. Doping is the process of addition of small amounts of certain specific impurity atoms having valency different from that of host atoms to a pure semiconductor. Doping is done to increase the number of mobile electrons/holes and hence to increase the conductivity of a semiconductor.

Problem 12. Why is *p*-type semiconductor so called ?

Solution. Because it has holes, the positive charge carriers, as the majority charge carriers.

Problem 13. Why is *n*-type semiconductor so called ?

Solution. Because it has electrons, the negative charge carriers, as the majority charge carriers.

Problem 14. What is a hole ? Which type of doping creates a hole ? [Himachal 03]

Solution. A hole is a vacant state in the covalent bond of a semiconductor from which an electron has been removed. When semiconductor is doped with trivalent impurity atoms of B, Al or In ; holes are created.

Problem 15. Carbon and silicon are known to have similar lattice structures. However, the four bonding electrons of carbon are present in second orbit while those of silicon are present in its third orbit. How does this difference result in a difference in their electrical conductivities ? [CBSE Sample Paper 08]

Solution. The energy required to take out an electron from Si atom is much smaller than that in case of C atom. Hence the number of free electrons for conduction is Si is quite significant but negligibly small for C. Consequently the conductivity of silicon is much greater than that of carbon.

Problem 16. **How is a sample of an *n*-type semiconductor electrically neutral though it has an excess of negative charge carriers ?** [CBSE SP 08 ; Haryana 10]

Solution. In an *n*-type semiconductor, the pentavalent impurity atom shares four of its valence electrons with four teletravalent host atoms while its fifth electron remains free. This impurity atom as a whole is electrically neutral. So the semiconductor is also neutral.

Problem 17. **Why is germanium preferred over silicon for making semiconductor devices ?**

Solution. This is because the energy gap for Ge ($E_g = 0.7\,eV$) is smaller than the energy gap for Si ($E_g = 1.1\,eV$).

Problem 18. **How does the energy gap in an intrinsic semiconductor vary, when doped with a pentavalent impurity ?** [CBSE D 2000]

Solution. The energy gap decreases when a semiconductor is doped with a pentavalent impurity due to the creation of a donor energy level just below the bottom of the conduction band.

Problem 19. **Why is the conductivity of *n*-type semiconductor greater than that of the *p*-type semiconductor even when both of these have same level of doping ?** [CBSE OD 05C]

Solution. This is because under a given electric field, free electrons have higher mobility than holes.

Problem 20. **Why do Ge and Si behave as semiconductors ?**

Solution. The energy gaps in Ge and Si are of the order of 1 eV. Electrons can be easily excited from valence band to the conduction band to enable them to conduct electricity. So Ge and Si behave as semiconductors.

Problem 21. **Why are metallic conductors opaque ?**

Solution. This is because the free electrons absorb all the light energy incident on the metallic conductor and do not allow light to pass through it.

Problem 22. **Of the ionic, covalent, metallic and vander Wall's solids, which class is most likely to produce an insulator, a conductor and a semiconductor ?**

Solution. (*i*) The ionic and vander Wall's solids are usually insulators.

(*ii*) Metallic solids are good conductors.

(*iii*) Covalent solids are usually semiconductors.

Problem 23. **There are two solids *A* and *B*. Certain physical properties of a crystal of *A* show a variation with direction and its conductivity increases with increase in temperature, while the properties of *B* are isotropic and it is a bad conductor of electricity. What type of bondings do *A* and *B* have ?**

Solution. The solid *A* has covalent bonding and the solid *B* has ionic bonding.

Problem 24. **Is the ionization energy of an isolated free atom different from the ionization energy E_g for the atom in a crystalline lattice ?** [NCERT]

Solution. Yes, the ionization energy of an isolated atom is different from its value in crystalline lattice. This is because in the periodic crystal lattice, each bound electron is influenced by many neighbouring atoms.

Problem 25. **Why is a *p-n* junction also called a junction diode ?**

Solution. A *p-n* junction allows a large current to flow through it when forward biased and it offers a high resistance when it is reverse biased. This unidirectional property is similar to that of a vacuum diode. Hence *p-n* junction is also called a junction diode.

Problem 26. **Why does a potential barrier set up across a junction diode ?**

Solution. The accumulation of negative charges in the *p*-region and positive charges in the *n*-region sets up a potential difference across the junction. This is called potential barrier which opposes the diffusion of electrons and holes across the junction.

Problem 27. **Which type of biasing results in very high resistance of a *p-n* junction diode ? Draw a diagram showing this bias.** [CBSE Sample Paper 98]

Solution. Reverse biasing results in very high resistance of *p-n* junction diode.

Figure 14.137 shows a reverse biased *p-n* junction diode.

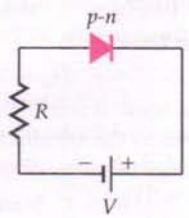


Fig. 14.137

Problem 28. **Can we measure the potential difference of a *p-n* junction by connecting a sensitive voltmeter across its terminals ?**

Solution. No, there are no free charge carriers in the depletion region. So it offers infinite resistance in the absence of any forward biasing.

Problem 29. **Why does the width of depletion layer of a *p-n* junction increase in reverse biasing ?** [CBSE OD 99]

Solution. During reverse biasing, the positive terminal of the external battery attracts electrons from the *n*-region and its negative terminal attracts holes from the *p*-region *i.e.*, the majority charge carriers move away from the junction. This increases the width of the depletion layer.

Problem 30. Can two *p-n* junction diodes placed back to back work as a *p-n-p* transistor ? [CBSE D 92C ; Punjab 03]

Solution. No. In that case the *n*-region forming the base will become quite thick and most of the majority charge carriers rushing from emitter to collector will get neutralised. The transistor will not work.

Problem 31. Why is the base region of a transistor made very thin and lightly doped ? [Himachal 96 ; CBSE D 02]

Solution. A thin and lightly doped base region contains a smaller number of majority charge carriers. This reduces the recombination rate of electrons and holes at the base-emitter junction. Most of the majority charge carriers coming from emitter into base immediately get collected by the collector. This reduces base current and increases both collector current and current gain of the transistor.

Problem 32. If the base region of a transistor is made large, as compared to a usual transistor, how does it affect (*i*) the collector current, and (*ii*) current gain of this transistor ? [CBSE OD 2000]

Solution. If the base region is made large, most of the charge carriers coming from the emitter would get neutralised in the base by the electron-hole recombination process and this will (*i*) reduce collector current and hence (*ii*) reduce current gain.

Problem 33. In the working of a transistor, the emitter-base (EB) junction is forward biased while collector-base (CB) junction is reverse biased. Why ? [CBSE 04C]

Solution. Only forward biased emitter-base junction can send the majority charge carriers from emitter to base and only reverse biased collector can collect these majority charge carriers from the base region. If the emitter is reverse biased, no charge carriers will flow towards the collector and hence no current will flow through the transistor.

Problem 34. Can we interchange emitter and collector of a transistor ?

Solution. No. We cannot interchange emitter and collector due to two reasons :

(*i*) The doping level of emitter is higher than that of collector.

(*ii*) The contact area of emitter-collector junction is larger than that of emitter-base junction.

Problem 35. A transistor is a temperature sensitive device. Comment.

Solution. When a transistor is properly biased, its electrons and holes carry current. If its temperature is increased, many of its covalent bonds may break producing a large number of extra electron-hole pairs which will set a large current through the transistor. This may produce a large amount of heat resulting in the complete breakdown of the transistor.

Problem 36. A transistor is a current operated device. Comment.

Solution. In a transistor, the collector current is controlled by the base current which is a part of emitter current. The changes in the emitter current are proportional to the changes in the base current and not to the input(base) voltage. Thus a transistor is a current operated device.

Problem 37. By increasing the load resistance, can we increase the voltage gain ($A_V = -g_m R_L$) of an amplifier indefinitely ?

Or

Explain the effect of increasing load resistance R, on the voltage gain of a transistor amplifier. [CBSE D 98C]

Solution. Initially, the voltage gain ($A_V = -g_m R_L$) increases with the increase in load resistance R_L.

But the gain of an amplifier cannot be increased indefinitely by increasing R_L. We know that

$$V_{CE} = V_{CC} - I_C R_L$$

If we increase R_L, V_{CE} decreases and if V_{CE} becomes less than V_{BE}, both the junctions get forward biased and saturation starts.

Problem 38. Why is a common emitter amplifier preferred over a common base amplifier ? [CBSE OD 97]

Solution. Because the current gain of common emitter amplifier is more than that of a common base amplifier.

Problem 39. When is a common base amplifier preferred over a common emitter amplifier ? [CBSE OD 97 ; D 07C]

Solution. When voltage amplification of the given signal is required without any phase change of signal voltage, common base transistor is preferred over common emitter amplifier.

Problem 40. What happens in a transistor when both the emitter and collector are reverse biased ? What is this condition known as ?

Solution. When both the emitter and collector are reverse biased, no current flows through the transistor as there is no conduction due to majority charge carriers across the emitter-base or collector-base junction. This condition is known as cut-off state.

Problem 41. Under what condition a transistor works as an open switch ?

Solution. A transistor works as an open switch in the cut-off state *i.e.*, when both the emitter and collector are reverse biased.

Problem 42. What happens in a transistor when both the emitter and collector are forward biased ? How will the collector current change if the emitter voltage is slightly increased ?

Solution. The transistor will be in the saturation state and it will not function as an amplifier. When the emitter voltage is slightly increased, the collector current does not change.

Problem 43. **Why a transistor cannot be used as a rectifier ?** [Punjab 91]

Solution. To use a transistor as a rectifier, either its emitter-base portion or collector base portion has to be used. As base is thin and lightly doped, either of the two portions will not work as a *p-n* junction. So a transistor cannot be used as a rectifier.

Problem 44. **Transistors do not work satisfactorily when used inside the railway carriage. Why ?**

Solution. The iron frame of railway carriage acts as a magnetic screen. It does not allow the e.m. wave signals coming from transmitter to enter the carriage. So a transistor cannot work satisfactorily inside a railway carriage.

Problem 45. **Is the voltage gain of a *CE* amplifier constant irrespective of the magnitude of the input signal ? Give reason.**

Solution. No. The voltage gain is constant for a limited range of input signal V_i. During the positive half-cycle, base current I_B increases which increases collector current I_C. If the increase in I_C is so large that V_{CE} becomes less than V_{BE}, the transistor goes into saturation state. Therefore, when

$$\beta I_B > I_C$$

the transistor does not work as an amplifier.

Problem 46. **In a transistor, the forward bias is always smaller than the reverse bias. Why ?**

Solution. If we apply a large forward biasing across the emitter, the majority charge carriers would move from emitter to collector through the base with a high velocity. This would produce excessive heating which would damage the transistor.

Problem 47. **How would you test in a simple way whether the transistor is spoiled or in working order ?** [Punjab 02]

Solution. For a transistor in working order, the forward biased emitter-base junction has a low resistance while the reverse biased base-collector junction has a high resistance. In a spoiled transistor, the resistance is low (or the path is conducting) in both situations.

Problem 48. **If the emitter and the base of a transistor have same doping concentration, how will the base current and collector current be affected ?**

Solution. When the base has same doping concentration as the emitter, the rate of recombination of electrons and holes increases as the majority charge carriers flow across the emitter-base junction. Consequently, the base current increases and collector current decreases.

Problem 49. **Which one of the transistors *p-n-p* and *n-p-n* is more useful and why ?**

Solution. *n-p-n* transistor is more useful than *p-n-p* transistor. In *n-p-n* transistor, electrons are the main charge carriers while in *p-n-p* transistor, holes are the main charge carriers. But electrons have higher mobility than holes. So *n-p-n* transistors are more commonly used than *p-n-p* transistors.

Problem 50. **Why is the area of the base-collector junction is made larger than the area of the emitter base junction in a transistor ?**

Solution. When a transistor works, most of the heat is produced at the base-collector junction. The area of this junction is made large so as to dissipate this heat.

Problem 51. **Why is a logic gate so called ?**

Solution. This is because a logic gate follows a certain logical relationship between input and output voltages.

Problem 52. **Why is a NOT gate known as an inverter ?**

Solution. A NOT gate always inverts the input. If input is low (0), the output is high (1) and vice versa. Hence a NOT gate is known as an inverter.

Problem 53. **How is a NOT gate different from AND or OR gate ? Can it be made from junction diodes ?**

Solution. AND and OR gates can have two or more inputs while a NOT gate has only one input. A NOT gate cannot be made from junction diodes. It is realised by using a transistor.

Problem 54. **Why are the NAND and NOR gates known as digital building blocks or universal gates ?**

Solution. The repeated use of NAND or NOR gates alone can give all other gates like OR, AND and NOT gates. In digital circuits the NAND or NOR gates serve as building blocks and hence they are named so.

Problem 55. **In the circuits shown in Fig. 14.138, a switch which is open represents the logic state 0 and the switch which is closed represents the logic state 1. The lamp *L* is lit when output is logic state 1. What types of gate are represented by the circuits in (*a*) and (*b*) ?** [CBSE OD 95]

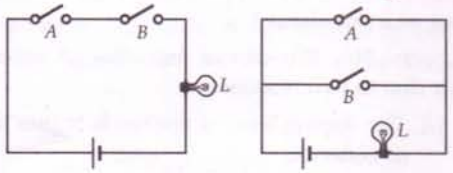


Fig. 14.138 (*a*) (*b*)

Solution. (*i*) The circuit in Fig. 14.138(*a*) represents an AND gate because the lamp *L* will glow only when both the switches *A* AND *B* are closed.

(*ii*) The circuit in Fig. 14.138(*b*) represents an OR gate because the lamp *L* will glow when switch *A* OR switch *B* OR both switches are closed.

SHORT ANSWER CONCEPTUAL PROBLEMS

Problem 1. **Fill in the blanks using the word(s) from the list appended with each statement :**

(*i*) As the temperature rises, the resistance offered by metals _____ (increases, decreases)

(*ii*) The conduction band of an insulator is _____ empty. (partially, practically)

(*iii*) The semiconductors are _____ at absolute zero. (conductors, insulators)

(*iv*) The resistance of semiconductors _____ with increasing temperature. (decreases, increases)

(*v*) The forbidden energy gap in case of a semiconductor is _____ as compared to that of an insulator. (smaller, greater)

(*vi*) In an intrinsic semiconductor, the electron and hole concentrations are _____ (equal, unequal)

(*vii*) When a block of semiconductor is connected to a battery by a metallic wire, the current flow in the wire is due to the motion of _____ in the wire. (electrons, electrons and holes)

(*viii*) The doping of an intrinsic semiconductor with certain type of impurity atoms causes a/an _____ in its electric conductivity. (decrease, increase)

(*ix*) The movement of charge carriers from a region of higher concentration to a region of lower concentration is called _____ (drift, diffusion)

(*x*) When a battery is connected to a *p*-type semiconductor with metallic wire, the current in the semi-conductor is predominantly due to _____ (electrons, holes)

(*xi*) Thomson coefficient for a *p*-type semiconductor is _____ (positive, negative)

(*xii*) The drift velocity of electrons is expected to be _____ (equal to, greater than) that of holes.

(*xiii*) When two isolated atoms are brought close to each other such that the distance between them is _____ (comparable to, much larger than) lattice spacing, the _____ (energy bands, energy levels) of the outermost electrons are split into _____ (very large, very small) number of levels, called _____ (energy gap, energy bands).

(*xiv*) The energy band in solids is an outcome of _____ (Pauli's exclusion principle, Coulomb's law).

Solution. (*i*) increases, (*ii*) partially, (*iii*) insulators, (*iv*) decreases, (*v*) smaller, (*vi*) equal, (*vii*) electrons, (*viii*) increase, (*ix*) diffusion, (*x*) holes, (*xi*) negative, (*xii*) greater than, (*xiii*) comparable to, energy levels, very large, energy bands, (*xiv*) Pauli's exclusion principle.

Problem 2. **Why do semiconductors obey Ohm's law for only low fields ?**

Solution. The drift velocity of a charge carrier is proportional to electric field E.

$$v = \frac{eE}{m}\tau \quad i.e., \quad v \propto E$$

But v cannot be increased indefinitely by increasing E. At high speeds, relaxation time τ begins to decrease due to the increase in collision frequency. So drift velocity saturates at the thermal velocity ($v_{th} = 10^5\ \text{ms}^{-1}$) and becomes independent of electric field at higher values of E. At 300 K,

$$v_{th} = \left(\frac{3k_B T}{m}\right)^{1/2} = 10^5\ \text{ms}^{-1}$$

$$\tau = 10^{-12}\text{s}$$

An electric filed of $10^6\ \text{Vm}^{-1}$ causes saturation of drift velocity. Hence semiconductors obey Ohm's law for low electric fields ($E < 10^6\ \text{Vm}^{-1}$) and above this field I becomes independent of V.

Problem 3. **Explain the variation of resistivity with temperature in pure-semiconductors.**

[CBSE F 93 C ; ISCE 97C]

Solution. The resistivity of a semiconductor is given by

$$\rho = \frac{1}{\sigma} = \frac{1}{e(n_e\mu_e + n_h\mu_h)}$$

As the temperature increases, the mobilities μ_e and μ_h of electrons and holes decrease due to the increase in their collision frequency. But due to the small energy gap of semiconductors, more and more electrons ($n \propto e^{-E_g/k_BT}$) from the valence band cross over to the conduction band. The increase in carrier concentrations, n_e and n_h is so large that decrease in the values of μ_e and μ_h has no influence. The overall effect is that conductivity increases or resistivity decreases with the increase of temperature.

Problem 4. **Distinguish between 'intrinsic' and 'extrinsic' semiconductors.** [CBSE D 15]

Solution.

	Intrinsic Semiconductor	Extrinsic Semiconductor
1.	Pure semiconductors not doped with any impurity atoms	Semiconductors doped with trivalent or penta-valent impurity atoms.
2.	$n_e = n_h$	$n_e \neq n_h$

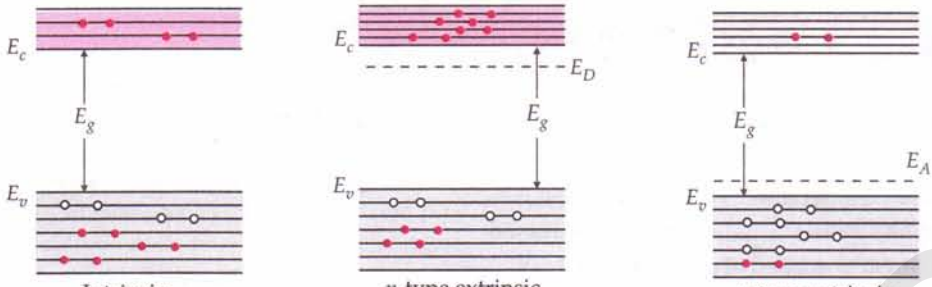


Fig. 14.139

Problem 5. Write any two distinguishing features between conductors, semiconductors and insulators on the basis of energy band diagrams. [CBSE D 14]

Solution. See Fig. 14.10 on page 14.7.

Distinguishing features on the basis of energy band diagrams :

Conductors	Semiconductors	Insulators
1. Either the conduction band is partially filled or the valence and conduction bands partly overlap. $E_g = 0$	Valence and conduction bands are separated by a small energy gap. E_g = 0.2 eV to 3 eV	Valence and conduction bands are separated by a large energy gap. $E_g > 3$ eV
2. They have large number of free electrons in the conduction band available for conduction.	They have a very small number of free electrons in the conduction band available for conduction.	They have no free electrons in the conduction band and so do not conduct electricity.

Problem 6. Distinguish between *n*-type and *p*-type semi-conductors on the basis of energy band diagrams. Compare their conductivities at absolute zero temperature and at room temperature. [CBSE D 15C]

Solution. See Figs 14.139(*b*) and (*c*) above.

n-type Semiconductors	*p*-type Semiconductors
1. An extra energy level, called donor level, lies just below the bottom of the conduction band.	An extra energy level, called acceptor level, lies just above the top of the valence band.
2. Most of the electrons come from the donor impurity.	Most of the holes are due to the acceptor impurity.
3. n_e(CB) >> n_h(VB)	n_h(VB) >> n_e(CB)

At absolute zero temperature, the conductivities of both *n*-type and *p*-type semiconductors are zero.

At room temperature, an equally doped *n*-type semiconductor will have more conductivity than a *p*-type semiconductor.

Problem 7. Draw the energy band diagram of (*i*) *n*-type (*ii*) *p*-type semiconductor at temperature, $T > 0$K.

In the case *n*-type Si semiconductor, the donor level is slightly below the bottom of conduction band whereas in *p*-type semiconductor, the acceptor energy level is slightly above the top of the valence band. Explain, what role do these energy levels play in conduction and valence bands. [CBSE OD 15C]

Solution. See Figs. 14.139 (*b*) and (*c*).

Conduction in *n*-type semiconductors : Role of donor level. The electrons from the donor atoms jump to the empty energy levels of the conduction band with very small supply of energy. So the conduction band has electrons as the majority charge carriers. When an external electric field is applied, these electrons drift in the opposite direction of the field.

Conduction in *p*-type semiconductors : Role of acceptor levels. With a very small supply of energy, the electrons from the valence band jump to acceptor energy level leaving behind holes in the valence band. When an electric field is applied, electrons from the neighbouring covalent bonds move into these holes, creating new holes in the direction of the field. Thus the holes act as positive charge carriers in the valence band.

Problem 8. What are donor and acceptor energy levels ?

Solution. **Donor energy levels.** In case of a *n*-type semiconductor, when a pentavalent donor atom replaces a Ge or Si atom, four of its five valence electrons form covalent bonds with the neighbouring Ge or Si atoms. The

fifth electron revolving around the nucleus of the donor atom requires very small energy (0.01 eV in Ge and 0.05 eV in Si) to leave the donor atom (because of high dielectric constant of Ge or Si). It occupies a discrete energy level just below the bottom of the conduction band. Such an energy level is called a donor energy level.

Acceptor energy level. In case of a *p*-type semiconductor, the trivalent acceptor atoms create holes which introduce energy levels just above the valence band (0. 01 eV above E_v in Ge and 0. 05 eV above E_v in Si). Such energy levels are called acceptor energy levels.

Problem 9. **The energy of a hole is higher, the farther below it is from the top of the valence band. Give reason.**

Solution. Imagine an electron being removed from the filled valence band to the bottom of the conduction band. This removal creates a vacancy or a hole in the valence band. Clearly, it requires more energy to remove an electron which is farther from the top of the valence band. Thus a valence hole state, farther from the top of the valence band, has higher energy just as a conduction electron farther from the bottom of the conduction band has higher energy.

Problem 10. **Distinguish between an intrinsic semiconductor and *p*-type semiconductor. Give reason, why, a *p*-type semiconductor crystal is electrically neutral, although $n_h >> n_e$?** [CBSE D 08, F 13]

Solution. The pure semiconductors (Ge or Si) in which the electrical conductivity is totally governed by electrons thermally excited from the valence band to the conduction band are called intrinsic semiconductors. They have equal number densities of free electrons and holes.

A tetravelent semiconductor of Si or Ge doped with trivalent impurity atoms of B, Al or In is called a *p*-type semiconductor. It has $n_h >> n_e$.

In a *p*-type semiconductor, the trivalent impurity atom shares its three valence electrons with the three tetravelent host atoms while the fourth bond remains unbonded. The impurity atom as a whole is electrical neutral. Hence the *p*-type semiconductor is also neutral.

Problem 11. **C, Si and Ge have same lattice structure. Why is C insulator while Si and Ge intrinsic semiconductors ?**

Solution. The 4 bonding electrons of C, Si or Ge lie, respectively, in the second, third and fourth orbit. Hence, the energy required to take out an electron from these atoms (*i.e.*, ionisation energy E_g) will be least for Ge, followed by Si and highest for C. Hence, the number of free electrons for conduction in Ge and Si are quite significant but negligibly small for C.

Problem 12. **Fill in the blanks using the word(s) from the list appended with each statement :**

(*i*) When a *p-n* junction is forward biased, then the motion of charge carriers across the barrier is due to _____ (drift, diffusion) and when it is reverse biased, then the motion of charge carriers is due to _____ (drift, diffusion).

(*ii*) An ideal *p-n* junction diode conducts, when _____ biased and does not conduct, when _____ biased.
(forward, reverse ; forward, reverse)

(*iii*) The base of a transistor is always _____ and _____ doped, compared to the emitter and collector. (thinner, thicker ; lightly, heavily)

(*iv*) In a transistor, as long as $V_{CE} >> V_{BE}$, the I_C is almost _____ of V_{CE}.
(independent, proportional)

(*v*) For using a transistor as an amplifier, the base-emitter junction is _____ biased and the base collector junction is _____ biased. (forward, reverse ; forward, reverse)

(*vi*) An oscillator is nothing but an amplifier _____ feedback. (with, without)

(*vii*) In a digital circuit, diodes and transistors are operated by a 5 V supply. The 1 state will correspond to _____ (0 V, 5 V) and the 0 state to _____ (0 V, 5 V).

(*viii*) Digital circuits can be made by repititive use of _____ gates. (AND, NAND)

(*ix*) An output 1 is obtained in an AND gate, when _____ of the input terminals are at 1 state. (either, both)

(*x*) An output 1 is obtained in a NOR gate, when ____ input terminals are at 0 state. (either, both)

Solution. (*i*) diffusion, drift, (*ii*) forward, reverse, (*iii*) thinner, lightly, (*iv*) independent, (*v*) forward, reverse, (*vi*) with, (*vii*) 5 V, 0 V, (*viii*) NAND, (*ix*) both, (*x*) both.

Problem 13. **With the help of suitable diagram, describe briefly the two important processes involved in the formation of a *p-n* junction. Define the terms depletion region and potential barrier.** [CBSE OD 12, 15 ; F 15]

Solution. **Formation of depletion region and potential barrier in a junction diode.** Two important processes involved during the formation of *p-n* junction are diffusion and drift. Due to the concentration gradient across the *p*- and *n*-sides of the junction, holes diffuse from *p*-side to *n*-side and electrons diffuse from *n*-side to *p*-side of the junction. This movement of charge carriers gives rise to diffusion current across the *p-n* junction. This process leaves behind –ve acceptor ions on the *p*-side and +ve donor ions on the *n*-side of the junction. *The space charge region on either side of the junction which gets devoid of mobile charge carriers and has only immobile ions is called depletion layer.*

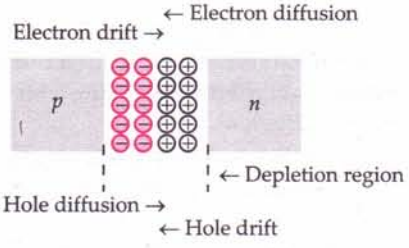


Fig. 14.140 Formation of *p-n* junction.

The accumulation of negative charges in the p-region and positive charges in the n-region sets up a potential difference across the junction. This is called barrier potential because it opposes the further diffusion of electrons and holes across the junction.

Problem 14. **An *n*-type semiconductor has excess of free electrons while a *p*-type semiconductor has a deficiency of these. But when a *p-n* junction is formed, all the electrons do not flow from *n*-region to the *p*-region. Why ?**

Solution. Though the *p*-type and *n*-type semiconductors have excess free electrons and holes respectively, yet they have equal number of fixed positive donor ions and negative acceptor ions respectively. When a *p-n* junction is formed, electrons diffuse from *n*-region to *p*-region while holes diffuse from *p*-region to *n*-region. As a result, the *n*-region near the junction becomes increasingly positive and the *p*-region becomes increasingly negative. This sets up a potential barrier across the junction which opposes the further diffusion of electrons and holes across the junction. That is why all the electrons do not flow from *n*-region to *p*-region.

Problem 15. **If a small voltage is applied to a *p-n* junction diode how will the barrier potential be affected when it is (*i*) forward biased, and (*ii*) reverse biased ? Briefly explain.** [CBSE D 05 ; OD 15]

Solution. (*i*) When *p-n* junction is forward biased, the positive terminal of the battery pushes the holes of *p*-region and negative terminal pushes the electrons of *n*-region towards the junction. The presence of electrons and holes decreases the width of the *p-n* junction, as shown in Fig. 14.141.

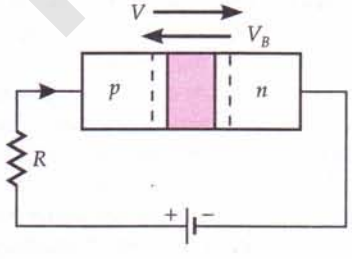


Fig. 14.141

(*ii*) When *p-n* junction is reversed biased, the negative terminal of the battery pulls holes from *p*-region and positive terminal pulls the electrons from the *n*-region away from the junction. This increases width of depletion layer, as shown in Fig. 14.142.

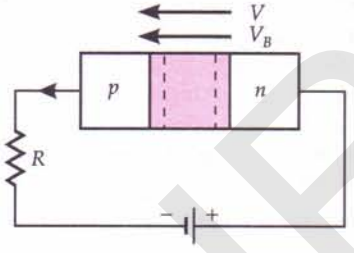


Fig. 14.142

Problem 16. **Draw a circuit diagram for *p-n* junction diode in forward bias. Sketch the voltage-current graph for the same.** [CBSE 93C, 95]

Solution. Figure 14.143 shows a forward biased *p-n* junction diode in which *p*-side is connected to the +ve terminal and *n*-side is connected to the –ve terminal of the battery and Fig. 14.144 shows its voltage-current graph.

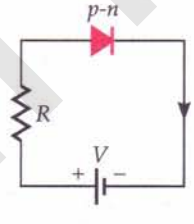


Fig. 14.143

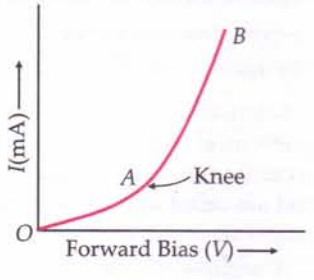


Fig. 14.144

Problem 17. **Draw a circuit diagram for the reverse biased *p-n* junction diode. Sketch the voltage-current graph for the same.**

Solution. Figure 14.145 shows a reverse biased *p-n* junction diode in which *p*-side is connected to the –ve terminal and *n*-side is connected to the +ve terminal of the battery and Fig. 14.146 shows its voltage-current graph.

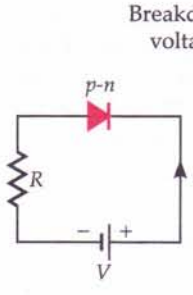


Fig. 14.145

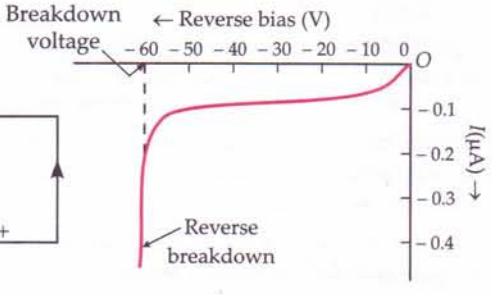


Fig. 14.146

Problem 18. **How is forward biasing different from reverse biasing in a *p-n* junction ?** [CBSE D 11]

Solution.

	Forward biasing of *p-n* junction	Reverse biasing of *p-n* junction
(*i*)	*p*-side is connected to the +ve terminal and *n*-side to the –ve terminal of the battery.	*p*-side is connected to the –ve terminal and *n*-side to the +ve terminal of the battery.
(*ii*)	Forward current is due to majority charge carriers.	Reverse current is due to minority charge carriers.
(*iii*)	Depletion layer becomes thin.	Depletion layer becomes thicker.
(*iv*)	Resistance across the *p-n* junction decreases.	Resistance across the *p-n* junction increases.

Problem 19. **In the following diagrams, indicate which of the diodes are forward biased and which are reverse biased.** [CBSE D 97 ; OD 02]

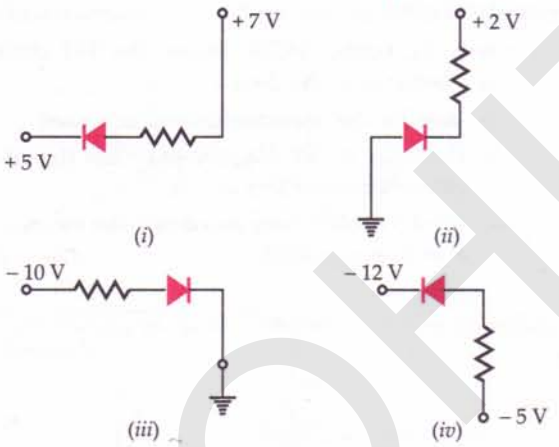


Fig. 14.147

Solution. (*i*) Forward biased, because *p*-side is at higher potential (+ 7 V) than *n*-side (+ 5 V).

(*ii*) Reverse biased, because *p*-side is at lower potential (0 V) than *n*-side (+ 2 V).

(*iii*) Reverse biased, because *p*-side is at lower potential (–10 V) than *n*-side (0 V).

(*iv*) Forward biased, because *p*-side is at higher potential (– 5 V) than *n*-side (– 12 V).

Problem 20. **Fig. 14.148 shows two *p-n* junction diodes along with a resistance *R* and a d.c. battery *E*. Indicate the path and direction of flow of appreciable current in the circuit.** [ISCE 98]

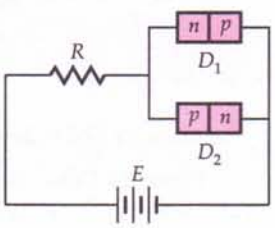


Fig. 14.148

Solution. In the given circuit, D_1 is reverse biased and does not conduct while D_2 is forward biased and conducts current. So a current flows along the path $E \rightarrow R \rightarrow D_2 \rightarrow E$.

Problem 21. **In the following circuits, if the input waveform is as shown in the figure, what will be the output wavefrom, (*i*) across *R* in Fig. 14.149(*a*), and (*ii*) across the diode in Fig. 14.149(*b*) ? Assume that the diode is ideal.**

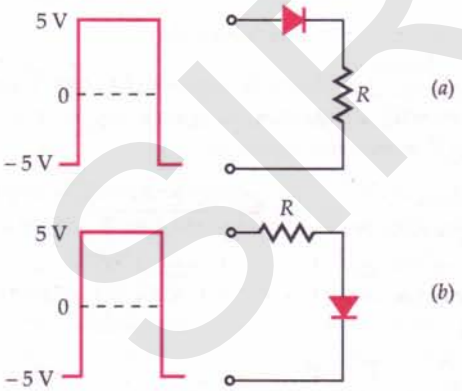


Fig. 14.149

Solution. (*i*) When the input level is – 5 V, the diode gets reverse biased. No output is obtained across *R*. When the input level becomes + 5 V, the diode gets forward biased and current flows through *R*. As the diode is ideal, the output across *R* will be exactly 5 V, as shown in Fig. 14.150(*a*).

Fig. 14.150

(*ii*) When the input level is – 5 V, the diode remains reverse biased. It does not conduct current. This part of the input wave appears across the diode, as shown in Fig. 14.150(*b*). When the input level is + 5 V, the diode gets forward biased and conducts currents. As the diode is ideal, no voltage appears across it.

Problem 22. **A square wave (– 1 V to 1 V) is applied to *p-n* junction diode as shown below. Draw the output waveform.** [ISCE 94]

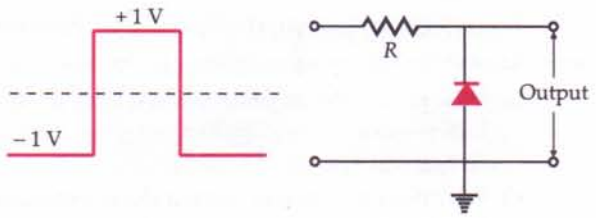


Fig. 14.151

Solution. The p-side of the diode is earthed, it is at zero potential. So the diode conducts current when input level is -1 V and does not conduct when the input level is $+1$ V. As the diode is ideal, the output across it will be either 0 or -1 V, as shown in Fig. 14.152.

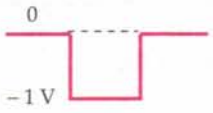


Fig. 14.152

Problem 23. **A diode is connected to 220 V (rms) a.c. in series with a capacitor, as shown below. What is the voltage V across the capacitor ?** [ISCE 96]

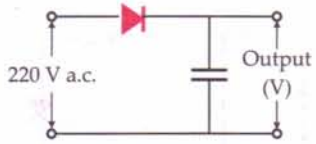


Fig. 14.153

Solution. During the positive half cycle of input a.c. (when the diode gets forward biased), the capacitor charges itself to the peak value of the supply voltage.

Therefore, the voltage across the capacitor is

$$V = V_0 = \sqrt{2}\, V_{rms} = \sqrt{2} \times 220 = \mathbf{311.1\ V}.$$

Problem 24. **How is it that the reverse current in a zener diode starts increasing suddenly at a relatively low breakdown voltage of 5 V or so ?** [CBSE OD 08C]

Solution. In a zener diode, both p-and n-sides are heavily doped with acceptor and donor impurities respectively. Due to this the depletion layer formed is very thin ($< 10^{-6}$ m). Even a small reverse bias voltage of 5 V sets up a very high electric field of 5×10^6 Vm^{-1}. This field is strong enough to pull valence electrons from the host atoms on the p-side which are accelerated to n-side. These electrons give rise to a large reverse current or breakdown current. *The emission of electrons from the host atoms due to high electric field is known as* ***internal field emission*** *or* ***field ionisation****. The breakdown of the diode due to internal field emission is called* ***zener breakdown****.*

Problem 25. **Draw V-I characteristics of a p-n junction diode. Answer the following questions, giving reasons :**

(*i*) Why is the current under reverse bias almost independent of the applied potential upto a critical voltage ?

(*ii*) Why does the reverse current show a sudden increase at the critical voltage ?

Name any semiconductor device which operates under the reverse bias in the breakdown region. [CBSE OD 13]

Solution. For V-I characteristic of a p-n junction diode, see Fig. 14.154.

(*i*) When the diode is reverse biased, a very small current of few μA flows due to the drift of minority charge carriers whose number density remains constant, so the current under reverse bias is almost independent of the applied potential upto a critical voltage.

(*ii*) When the reverse voltage across the p-n junction reaches a critical voltage, the reverse current suddenly increases to a large value. It is due to the increase in the number of minority charge carriers because of the breakdown of the diode. The avalanche breakdown occurs in lightly doped diodes due to ionisation by collision. Zener breakdown occurs at low voltages in heavily doped diodes by field emission.

Zener diode is the semiconductor device which operates under the reverse bias in the breakdown region.

Problem 26. **Figure 14.154 shows the V-I characteristic of a semiconductor diode.**

(*i*) Identify the semiconductor diode used.

(*ii*) Draw the circuit diagram to obtain the given characteristic of this device.

(*iii*) Briefly explain how this diode can be used as a voltage regulator. [CBSE D 08]

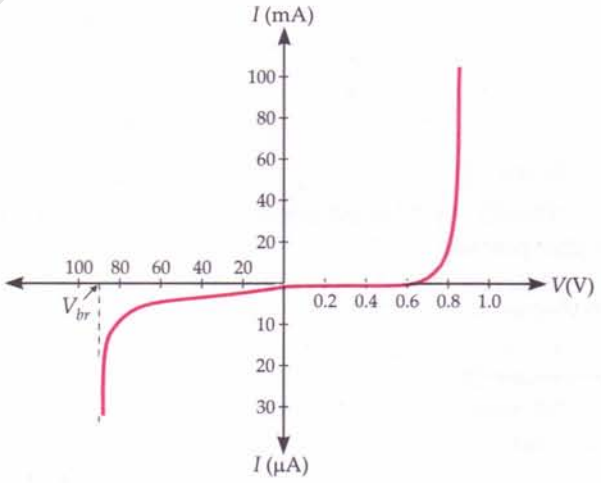


Fig. 14.154

Solution. (*i*) Zener diode.

(*ii*) Figure 14.155(*a*) shows circuit diagram for forward biasing and Fig. 14.155(*b*) for reverse biasing of Zener diode.

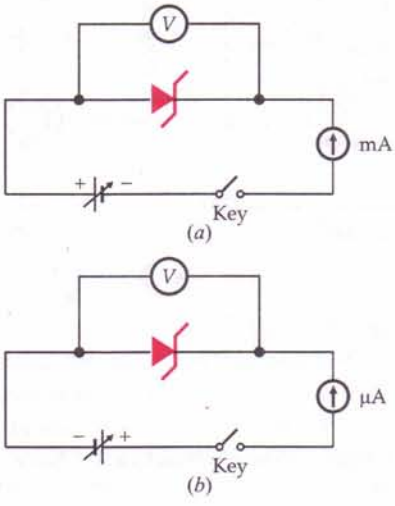


Fig. 14.155

(*iii*) Figure 14.156 shows the circuit diagram for using Zener diode as a voltage regulator.

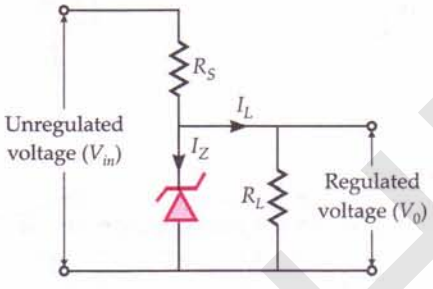


Fig. 14.156

When Zener diode is operated in the reverse breakdown region, the voltage across it remains practically constant (V_Z) for a large change in reverse current. So any increase/decrease of the input voltage results in, increase/decrease of the voltage drop across R_s without any change in voltage across Zener diode. Hence the Zener diode acts as a voltage regulator.

Problem 27. With what considerations in view, a photodiode is fabricated ? State its working with the help of a suitable diagram.

Even though the current in the forward bias is known to be more than in the reverse bias, yet the photodiode works in reverse bias. What is the reason ? [CBSE D 15]

Solution. The photodiode is fabricated with a transparent window so that light can fall on its *p-n* junction.

Working. See Fig. 14.35 on page 14.22.

When the photodiode is illuminated with photons of energy $h\nu > E_g$, additional electron-hole pairs are generated in or near the depletion region due to the absorption of photons. Due to the junction field, electrons get collected on *n*-side and holes on *p*-side which produces an emf. This sets up a photocurrent in the circuit, proportional to the intensity of incident light.

Reason. The fractional change in the minority carrier current, obtained under reverse bias, is much more than the corresponding fractional change in majority carrier current obtained under forward bias.

Problem 28. Mention the important considerations required while fabricating a *p-n* junction diode to be used as a Light Emitting Diode (LED). What should be the order of band gap of an LED if it is required to emit light in the visible range ? [CBSE D 13]

Solution. Important points of consideration for fabricating a *p-n* junction diode to be used as an LED :

1. It should be a heavily doped *p-n* junction diode.
2. The reverse breakdown voltages be very low for LEDs.
3. The semiconductor used for fabrication of visible LEDs must atleast have a band gap of 1.8 eV.

   For an LED to emit visible light, the order of band gap is 1.8 eV to 3 eV.

Problem 29. Distinguish between the light emitting diode and the photodiode. [CBSE Sample Paper 1998]

Solution. Difference between light emitting diode and photodiode :

Light Emitting Diode(LED)	Photodiode
1. It is forward biased.	It is reverse biased.
2. Recombination of electrons and holes takes place at the junction and emits e. m. radiation.	Energy ($h\nu$) is supplied by light to take an electron from valence band to conduction band.

Problem 30. What do the acronyms 'LASER' and 'LED' stand for ? Name the factor which determines (*i*) frequency, and (*ii*) intensity of light emitted by LED. [CBSE D 05C]

Solution. LASER stands for light amplification by stimulated emission of radiation ; LED stands for light emitting diode.

(*i*) The frequency of light emitted by an LED depends on the band gap of the semiconductor used in LED.

(*ii*) The intensity of light depends on the doping level of the semiconductor used.

Problem 31. Explain why the input resistance of a transistor is low while the output resistance is high.

Solution. The input (emitter) circuit of a transistor is always forward biased and the output (collector) circuit is reverse biased. Consequently, a smaller variation of input voltage produces a large variation in the input emitter current. This implies that the input resistance of a transistor is very low.

The reverse biased collector collects all the charge carriers that diffuse into it through the base. Consequently, a very large change in the collector voltage produces only a small change in the collector current. This implies that the output resistance of the transistor is very high.

Problem 32. **In the *n-p-n* transistor circuit shown in Fig. 14.157, what is the base to collector voltage ? What are the biasings (forward or reverse) of the emitter-base and the base-collector junctions ?**

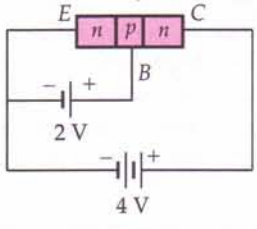


Fig. 14.157

Solution. Base to collector voltage

$$= 4 - 2 = \mathbf{2\ V}$$

$V_{EB} = \mathbf{2\ V}$ (Forward)

$V_{BC} = \mathbf{2\ V.}$ (Reverse)

Problem 33. **Name the type of biasing which results in very high resistance of a *p-n* junction diode. In the given circuit, a voltmeter '*V*' is connected across a bulb '*B*'. What changes would occur in bulb '*B*' and voltmeter '*V*', if the resistor '*R*' is increased in value ? Give reason for your answer.** [CBSE D 02C]

Solution. The reverse biasing results in very high resistance across the *p-n* junction.

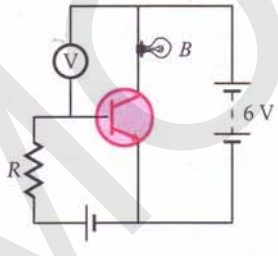


Fig. 14.158

If the value of the resistance *R* is increased, the current in the forward biased input circuit decreases. The emitter current I_E decreases and hence the collector current ($I_C = I_E - I_B$) also decreases. The glowness of the bulb decreases. Due to decrease in I_C, the potential drop across the bulb *B* decreases and hence the voltmeter shows a lower voltage.

Problem 34. **In only one of the circuits given in Fig. 14.159, the lamp *L* lights. Which circuit is it ? Give reason for your answer.**

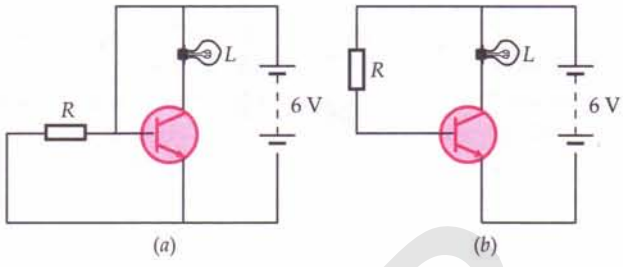


Fig. 14.159

Solution. The lamp *L* lights in the circuit of Fig. 14.159(*b*) because in this circuit, the input circuit is forward biased and the output circuit is reverse biased.

Problem 35. **In only one of the circuits given below the lamp *L* lights. Which circuit is it ? Give reason for your answer.** [CBSE D 01C]

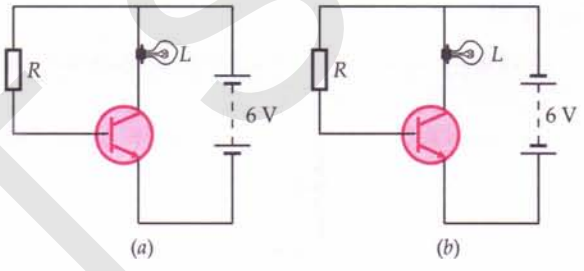


Fig. 14.160

Solution. The lamp *L* lights up only in the circuit of Fig. 14.160(*a*) because in this circuit, the input circuit is forward biased and the output circuit is reverse biased.

Problem 36. **In the given circuit diagram, a voltmeter '*V*' is connected across a lamp '*L*'. How would (*i*) the brightness of the lamp and (*ii*) voltmeter reading '*V*' be affected, if the value of resistance '*R*' is decreased ? Justify your answer.** [CBSE OD 01C ; D 13]

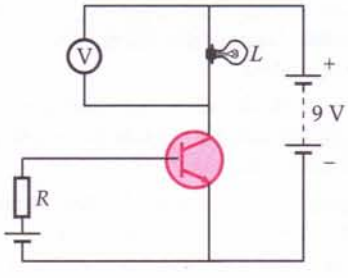


Fig. 14.161

Solution. (*i*) If the value of the resistance *R* is reduced, the current in the forward biased input circuit increases. The emitter current I_E and the collector current I_C ($I_C = I_E - I_B$) both increase. The lamp *L* glows more brilliantly. (*ii*) Due to the increase in I_C, the potential drop across the lamp *L* increases and hence the voltmeter *V* indicates a higher voltage.

Problem 37. **In the amplifier, the voltage applied at the input resistance r_i is amplified to give an output voltage $A_v v_i$. An a.c. input voltage is connected with a capacitor in series at the input terminals as shown in the Fig. 14.162.**

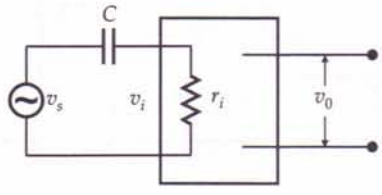


Fig. 14.162

Which of the following figures give the correct variation of the magnitude of output voltage as a function of the frequency ? (v_s does not change with frequency) [NCERT]

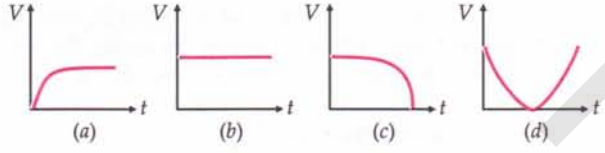


Fig. 14.163

Solution. Figure 14.163(*a*) gives the correct variation of the magnitude of output voltage as a function of frequency. This is because the capacitor offers a reactance X_C, given by

$$X_C = \frac{1}{2\pi f C}$$

For small values of f, X_C is high and, therefore

$$v_i = \frac{v_s}{X_C}$$

is low. As f increases, X_C decreases. This in turns, increases v_i and hence output voltage

$$v_0 = A_v . v_i$$

also increases. At a certain value of f, X_C becomes negligible, v_i becomes nearly equal to v_s and then v_0 becomes constant.

Problem 38. **What is an amplifier ? Can a transistor amplifier generate power ?**

Solution. An amplifier is a circuit consisting of atleast one transistor which can be used to increase current, voltage or power of alternating form. No. It cannot generate power. The energy for the higher a.c. power at the output is obtained from the d.c. battery.

Problem 39. **(*a*) Differentiate between three segments of a transistor on the basis of their size and level of doping.**

(*b*) When is a transistor said to be in active state ?

(*c*) Draw a plot of transfer characteristic (V_0 *vs.* V_i) and show which portion of the characteristic is used in amplification and why ?

(*d*) Draw the circuit diagram of base bias transistor amplifier in CE configuration and briefly explain its working. [CBSE D 14, 15 ; OD 15, 15C]

Solution. (*a*) **Emitter.** It is of moderate size and heavily doped semiconductor.

Base. It is very thin and lightly doped.

Collector. It is moderately doped and larger in size than the emitter.

(*b*) A transistor is said to be in active state when its emitter-base junction is forward biased and the base-collector junction is reverse biased. A Si transistor is in active state when its input (*E*-*B*) voltage is between 0.6 V and 1.0 V.

(*c*) A transfer characteristic is a graph of output voltage (V_0) *vs.* input voltage (V_i) for a base biased transistor. It is of the type as shown in Fig. 14.164.

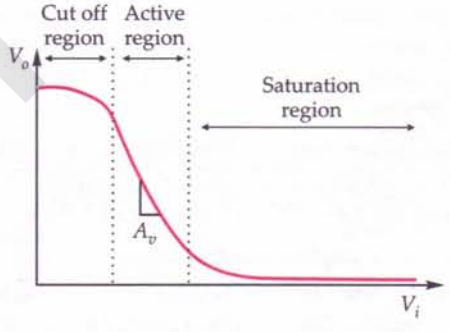


Fig. 14.164

The active region of the transfer characteristic is used for the amplification purpose. This is because in this region, I_C increases almost linearly with the increase of V_i.

(*d*) The circuit diagram for base biased *n*-*p*-*n* transistor amplifier, in CE configuration, is shown in Fig. 14.165.

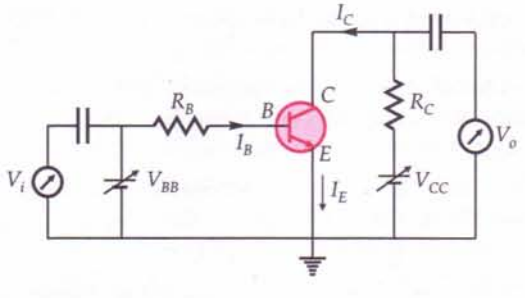


Fig. 14.165

Working. When a small sinusoidal voltage is superposed on the dc base bias, the base current will have sinusoidal variations superposed on the value of I_B. As a consequence, the collector current also will have sinusoidal variations superposed on the value of I_C. The output, between the collector and the ground, will be an amplified version of the input sinusoidal voltage.

Problem 40. **Give reasons for the following :**

(*i*) The Zener diode is fabricated by heavily doping both the *p*- and *n*- sides of the junction.

(*ii*) A photodiode, when used as a detector of optical signals is operated under reverse bias.

(*iii*) The band gap of the semiconductor used for fabrication of visible LEDs must atleast be 1.8 eV. [CBSE SP 15]

Solution. (*i*) Heavy doping makes the depletion region very thin. This makes the electric field of the junction very high, even for a small reverse bias voltage. This in turn helps the Zener diode to act as a 'voltage regulator'.

(*ii*) When operated under reverse bias, the photodiode can detect changes in current with changes in light intensity more easily because the fractional change in minority charge carries is more than that in majority charge carriers.

(*iii*) The photon energy, of visible light photons, varies from about 1.8 eV to 3 eV. Hence for visible LEDs, the semiconductor must have a band gap of 1.8 eV.

Problem 41. **Explain the following :**

(*i*) In the active state of the transistor, the emitter-base junction acts as a low resistance while base-collector region acts as a high resistance.

(*ii*) Output characteristics are controlled by input characteristics in common emitter transistor amplifier.

(*iii*) LEDs are made of compound semiconductor and not of elemental semiconductions. [CBSE SP 2016]

Solution. (*i*) This is because the emitter-base junction is forward biased whereas base-collector junction is reverse biased.

(*ii*) Small change in the current I_B in the base circuit controls the larger current I_C in the collector circuit. $I_C = \beta I_B$.

(*iii*) The band gap in elemental semiconductors corresponds to the wavelengths in the infrared region. So they cannot be used for making LEDs.

Problem 42. **The graph of potential barrier $V(x)$ versus width x of depletion region for an unbiased diode is shown in Fig. 14.166. In contrast to graph *A*, the graphs *B* and *C* are obtained after biasing the diode in different ways. Identify the type of biasing in *B* and *C*. Justify your answer.** [CBSE Sample Paper 2016]

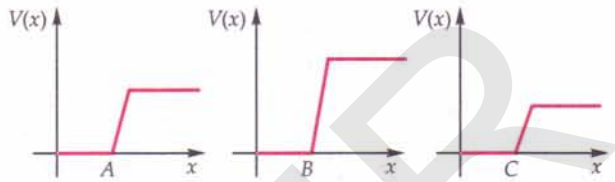


Fig. 14.166

Solution. *B* is reverse biased. The potential barrier increases in reverse biasing.

***C* is forward biased.** The potential barrier decreases in forward biasing.

Problem 43. **Give the symbol, and the truth table, of each of the two logic gates, obtained by using the two circuits, shown below.** [CBSE D 04C]

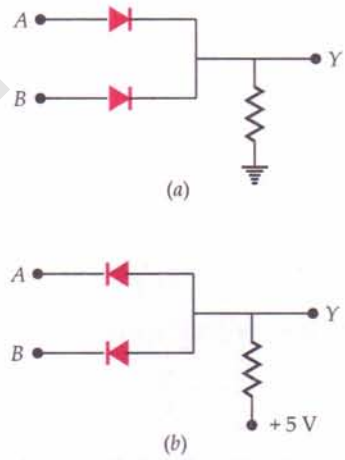


Fig. 14.167

Solution. (*a*) The circuit of Fig. 14.167(*a*) represents OR gate.

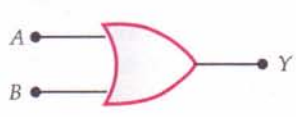


Fig. 14.168
Logic symbol of OR gate.

Truth table of OR gate

Input *A*	Input *B*	Output *Y*
0	0	0
0	1	1
1	0	1
1	1	1

(*b*) The circuit of Fig. 14.167(*b*) represents AND gate.

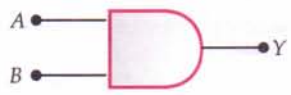


Fig. 14.169
Logic symbol of AND gate.

Truth table of AND gate

Input A	Input B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1

Problem 44. **Give the symbol, and the truth table of each of the two logic gates, obtained by using the two gate combinations, shown in Fig. 14.170.**

[CBSE D 04C, OD 15]

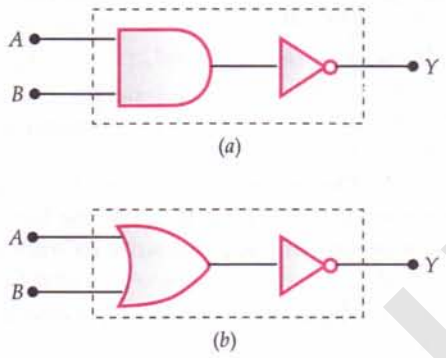


Fig. 14.170

Solution. (*a*) The gate combination of Fig. 14.170(*a*) represents a NAND gate.

Fig. 14.171
Logic symbol of NAND gate.

Truth table of NAND Gate

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

(*b*) The gate combination of Fig. 14.170(*b*) represents a NOR gate.

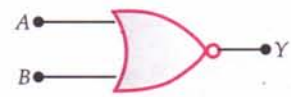


Fig. 14.172
Logic symbol of NOR gate.

Truth table of NOR gate

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

Problem 45. **(*i*) Sketch the output waveform from an AND gate for the inputs A and B shown in Fig. 14.173.**

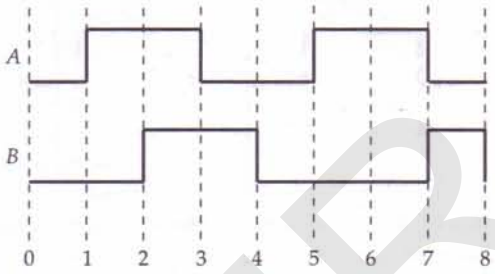


Fig. 14.173

(*ii*) If the output of the above AND gate is fed to a NOT gate, name the gate of the combination so formed.

[CBSE D 09]

Solution. (*i*) The output of an AND gate is 1 when both the inputs are 1. Hence the output waveform from the AND gate for the inputs A and B is of the type shown below :

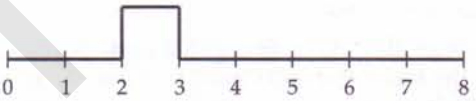


Fig. 14.174

(*ii*) A NAND gate is obtained when the output of an AND gate is fed to a NOT gate.

Problem 46. **Name the 2-input logic gate, whose truth table is given below :**

A	B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

If this logic gate is connected to a NOT gate, what will be the output when (*i*) $A = 1, B = 1$ and (*ii*) $A = 0, B = 1$?

[CBSE OD 03C]

Solution. As $Y = \overline{AB}$, so the given truth table is for a NAND gate.

Input A	Input B	Output of NAND gate, Y	Output of NOT gate $= \bar{Y}$
1	1	0	1
0	1	1	0

Problem 47. **Draw the logic symbol of the gate whose truth table is given below :**

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If this logic gate is connected to NOT gate, what will be the output when (*i*) $A = 0, B = 0$ and (*ii*) $A = 1, B = 1$? Draw the logic symbol of the combination.

[CBSE OD 03C ; F 09]

Solution. The given truth table is for a NOR gate.

Its logic symbol is shown in Fig. 14.172.

Inputs		Output of NOR gate	Output of NOT Gate
A	B	Y	$\bar{Y}$
0	0	1	0
1	1	0	1

The combination acts as an OR gate. Its logic symbol is shown in Fig. 14.168.

Problem 48. **If the output of a 2-input NAND gate is fed as the input to a NOT gate, (*i*) name the new logic gate obtained and (*ii*) write down its truth table.**

[CBSE OD 01, 02]

Solution.

Inputs		Output of NAND gate	Output of NOT gate
A	B	$Y' = \overline{A \cdot B}$	$Y = \bar{Y}'$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

As $Y = A \cdot B$, the new logic gate obtained is an AND gate.

Problem 49. **If the output of a 2-input NOR gate is fed as the input to a NOT gate (*i*) name the new logic gate obtained and (*ii*) write down its truth table.**

[CBSE OD 01, 02]

Inputs		Output of NOR gate	Output of NOT gate
A	B	$Y' = \overline{A + B}$	$Y = \bar{Y}'$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Solution. As $Y = A + B$, so the new logic gate obtained is an OR gate.

Problem 50. **The output of an AND gate is connected to both the inputs of a NAND gate. Draw the logic circuit of this combination of gates and write its truth table.**

[CBSE D 2000 C]

Solution. The logic circuit for the given combination of gates is shown below.

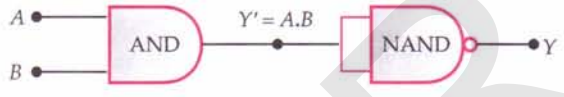


Fig. 14.175

Truth table

A	B	$Y' = A \cdot B$	$Y = \overline{Y' \cdot Y'}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Problem 51. **The output of an OR gate is connected to both the inputs of a NAND gate. Draw the logic circuit of this combination of gates and write its truth table.**

[CBSE D 2000C]

Solution. The logic circuit of the combination is shown below :

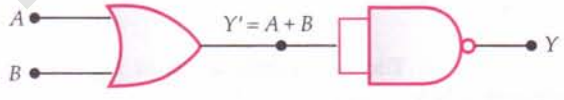


Fig. 14.176

Truth table

A	B	$Y' = A + B$	$Y = \overline{Y' \cdot Y'}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Problem 52. **Identify the logic gates marked *P* and *Q* in the given logic circuit. Write down the output at *X* for the inputs (*i*) $A = 0, B = 0$ and (*ii*) $A = 1, B = 1$.** [CBSE D 03C]

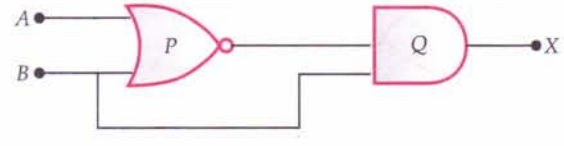


Fig. 14.177

Solution. The logic gate P is NOR gate and Q is AND gate.

Input A	Input B	Output of NOR gate $Y = A + B$	$X = B.Y$
0	0	1	0
1	1	0	0

Problem 53. **Identify the logic gates marked P and Q in the given logic circuit.**

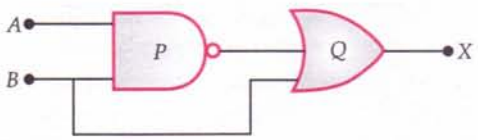


Fig. 14.178

Write down the output at X for the inputs (*i*) $A = 0$, $B = 0$ and (*ii*) $A = 1$, $B = 1$. [CBSE D 03C]

Solution. The gate P is NAND gate and gate Q is OR gate.

Input A	Input B	Output of NAND gate $Y = A . B$	Output of OR gate $X = B + Y$
0	0	1	1
1	1	0	1

Problem 54. **The following truth table gives the output of a 2-input logic gate :**

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

(*i*) Identify the logic gate used and draw its logic symbol.

(*ii*) If the output of this gate is fed as input to a NOT gate, name the new logic gate so formed. [CBSE OD 2000]

Solution. (*i*) The gate used is NAND gate. Its logic symbol is shown in Fig. 14.179.

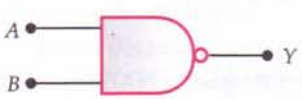


Fig. 14.179

(*ii*) When the output of NAND gate is fed to a NOT gate.

Input A	Input B	Output of NAND gate $Y' = \overline{A . B}$	Output of NOT gate $Y = \overline{Y'}$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Clearly, output $Y = A . B$. So the new logic gate formed is an AND gate.

Problem 55. **The following figure shows the input waveforms (A, B) and the output waveform (Y) of a gate. Identify the gate, write its truth table and draw its logic symbol.** [CBSE OD 06C ; D09]

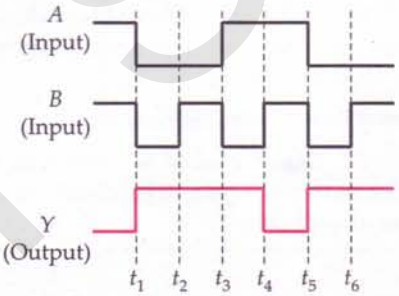


Fig. 14.180

Solution. Clearly, the output is low when both the inputs are high otherwise it is high. Hence it is a NAND gate. The truth table and logic symbol are given in Problem 54.

Problem 56. **The output of an OR gate is connected to both the inputs of a NOR gate. Draw the logic circuit of this combination of gates and write its truth table.** [CBSE F 94 C]

Solution. The logic circuit of the combination is shown in Fig. 14.181.

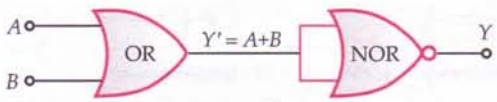


Fig. 14.181

Truth Table

A	B	Y'	$Y = \overline{Y' + Y'}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Problem 57. **The output of an AND gate is connected to both the inputs of a NAND gate. Draw the logic circuit of this combination of gates and write its truth table.** [CBSE OD 94 C]

Solution. The logic circuit of the combination is shown in Fig. 14.182.

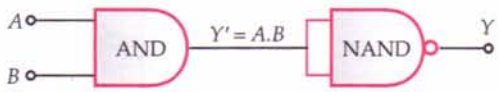


Fig. 14.182

Truth Table

A	B	$Y' = A.B$	$Y = \overline{Y'.Y'}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Problem 58. **Using a suitable combination from a NOR, an OR and a NOT gate, draw circuits to obtain the truth tables given below :** [CBSE Sample Paper 08]

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	0

(*i*)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	1

(*ii*)

Solution. To obtain the truth table (*i*), the circuit consisting of a NOR gate and a NOT as shown in Fig. 14.175(*a*) can be used.

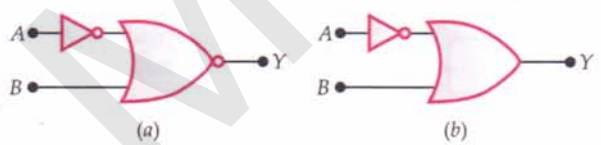


Fig. 14.183

To obtain the truth table (*ii*), the circuit consisting of an OR gate and a NOT gate as shown in Fig. 14.183(*b*) can be used.

Problem 59. **Draw the output waveform at X, using the given inputs A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit.** [CBSE D 08, 11]

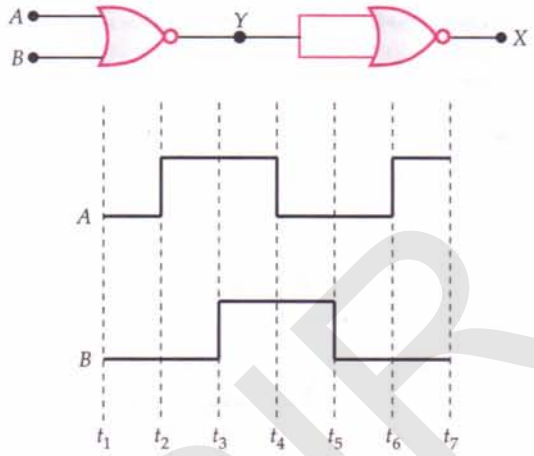


Fig. 14.184

Solution. $Y = \overline{A + B}$

$X = \overline{Y} = A + B$

Thus the given circuit performs OR operation. The output waveform obtained at X is of the type shown below.

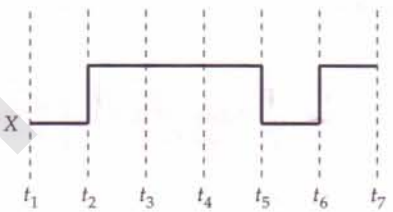


Fig. 14.185

Problem 60. **Draw the output waveform at X, using the given inputs A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit.** [CBSE D 11]

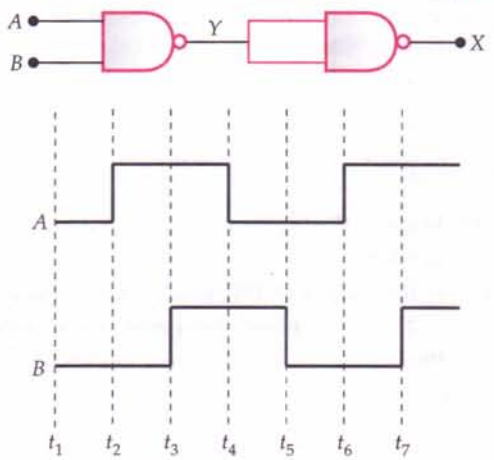


Fig. 14.186

Solution. The first gate is NAND gate. Its output Y is fed to a NOT gate (made from NAND gate).

$\therefore \quad Y = \overline{A.B}$ and $X = \overline{Y} = A.B$

Hence the given circuit performs the function of an AND gate. The output waveform obtained at X is of the type shown below.

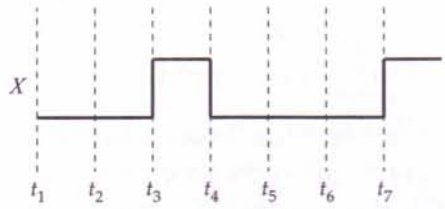


Fig. 14.187

Problem 61. **Inputs A and B are applied to the logic gate set up as shown below. Complete the truth table given below, and name the equivalent gate formed by this 'set-up'.** [CBSE D 13]

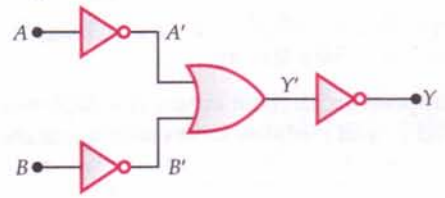


Fig. 14.188

A	B	A'	B'	Y
0	0			
0	1			
1	0			
1	1			

Solution. Truth table for the given circuit is as follows :

A	B	$A' = \bar{A}$	$B' = \bar{B}$	$Y' = \bar{A} + \bar{B}$	$Y = \bar{Y'}$
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

Clearly, $Y = A.B$.

Hence the given circuit is equivalent to an AND gate.

HOTS Problems on Higher Order Thinking Skills

Problem 1. *For the circuit shown in Fig. 14.189, find the current flowing through the 1Ω resistor. Assume that the two diodes, D_1 and D_2, are ideal diodes.* [CBSE D 13C]

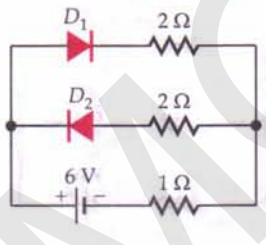


Fig. 14.189

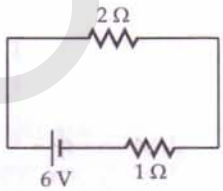


Fig. 14.190

Solution. Diode D_1 is forward biased and offers zero resistance.

Diode D_2 is reversed biased and offers infinite resistance.

The given circuit reduces to the equivalent circuit shown in Fig. 14.190.

By Ohm's law, the current through the 1Ω resistor is

$$I = \frac{6}{2+1}\text{A} = 2\text{ A}.$$

Problem 2. *Why is a photodiode operated in reverse bias mode ? Fig. 14.191 shows reverse bias current, under different illumination intensities I_1, I_2, I_3 and I_4, for a given photodiode. Arrange the intensities I_1, I_2, I_3 and I_4, in decreasing order of magnitude.* [CBSE Sample Paper 11]

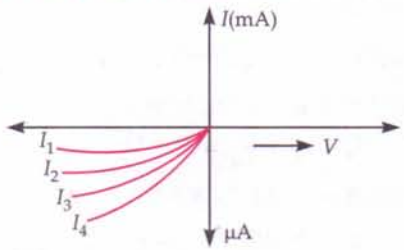


Fig. 14.191

Solution. Due to photo-effects, the fractional increase in minority charge carriers is more than the fractional increase in majority charge carriers, hence the fractional change on minority carrier dominated reverse bias current is more easily measurable.

As the reverse saturation current through a photodiode increases with the increase in intensity of incident radiation, so $I_4 > I_3 > I_2 > I_1$.

Problem 3. *Assume that the silicon diode in the circuit shown in Fig. 14.192 requires a minimum current of 1 mA to be above the knee point (0.7 V) of its I-V characteristics.*

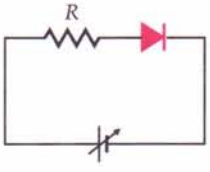


Fig. 14.192

Also assume that the voltage across the diode is independent of current above the knee point.

(*a*) *If $V_B = 5$ V, what should be the maximum value of R so that the voltage is above the knee point ?*

(*b*) *If $V_B = 5$ V, what should be the value of R to establish the current of 5 mA in the circuit ?*

(*c*) *What is the power dissipated in the resistance R and in the diode, when a current of 5 mA flows in the circuit at $V_B = 6$ V ?*

(*d*) *If $R = 1\,\text{k}\Omega$, what is the minimum voltage V_B required to keep the diode above the knee point ?*

Solution. When the minimum current of 1 mA flows through the circuit, the potential drop of 0.7 V occurs across the diode for a forward bias of 5 V.

(*a*) Here $V_B = 5$ V, $V_D = 0.7$ V, $I_{min} = 1\,\text{mA} = 10^{-3}$ A

Now $V_B = V_R + V_D$

or $5 = I_{min} \times R_{max} + 0.7$

or $5 - 0.7 = 10^{-3} \times R_{max}$

or $R_{max} = \dfrac{4.3}{10^{-3}} = \mathbf{4.3 \times 10^3\ \Omega}.$

(*b*) To establish a current of 5 mA in the circuit, we have

$V_B = 5$ V, $I = 5\,\text{mA} = 5 \times 10^{-3}$ A, $V_D = 0.7$ V

(which does not depend on current above knee point)

As $V_B = V_R + V_D = IR + V_D$

$\therefore \quad 5 = 5 \times 10^{-3} \times R + 0.7$

or $R = \dfrac{5 - 0.7}{5 \times 10^{-3}} = \dfrac{4.3}{5 \times 10^{-3}}\ \Omega = \mathbf{860\ \Omega}.$

(*c*) Here $V_B = 6$ V, $I = 5\,\text{mA} = 5 \times 10^{-3}$ A, $V_D = 0.7$ V

$\therefore \quad V_R = V_B - V_D = 6 - 0.7 = 5.3$ V

As power dissipated, $P = VI$

$\therefore$ Power dissipated in resistance R

$= V_R I = 5 \times 10^{-3} \times 5.3$ W

$= 26.5 \times 10^{-3}$ W $= \mathbf{26.5\ mW}$

Power dissipated in the diode

$= V_D I = 0.7 \times 5.3 \times 10^{-3}$ W

$= 3.5 \times 10^{-3}$ W $= \mathbf{3.5\ mW}$

(*d*) Here $R_{max} = 1\,\text{k}\Omega = 10^3\ \Omega$,

$I_{min} = 1\,\text{mA} = 10^{-3}$ A

$\therefore \quad V_B = V_R + V_D = I_{min} \times R_{max} + V_D$

$= 10^{-3} \times 10^3 + 0.7 = \mathbf{1.7\ V}.$

Problem 4. *A potential barrier of 0.50 V exists in a p-n junction. (i) If the depletion region is 5.0×10^{-7} m thick, what is the electric field in this region ? (ii) If an electron approaches the p-n junction from the n-side with a speed of 5×10^{-7} ms^{-1}, with what speed will it enter the p-side ?*

Solution. (*i*) Electric field,

$$E = \frac{V}{d} = \frac{0.50\ \text{V}}{5.0 \times 10^{-7}\ \text{m}} = \mathbf{1.0 \times 10^6\ Vm^{-1}}$$

(*ii*) Suppose an electron enters the depletion layer with speed v_1 and p-region with speed v_2, as shown in

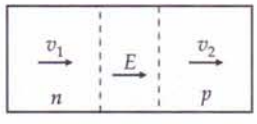


Fig. 14.193

Fig. 14.193. Its potential energy increases by eV joule. By energy conservation ;

$$\frac{1}{2} mv_2^2 + eV = \frac{1}{2} mv_1^2$$

or $$\frac{1}{2} mv_2^2 = \frac{1}{2} mv_1^2 - eV$$

$$= \frac{1}{2} \times 9.1 \times 10^{-31} (5.0 \times 10^5)^2 - 1.6 \times 10^{-19} \times 0.50$$

$$= (1.13 - 0.8) \times 10^{-19} = 0.33 \times 10^{-19}\ \text{J}$$

$\therefore \quad v_2^2 = \dfrac{2 \times 0.33 \times 10^{-19}}{m} = \dfrac{0.66 \times 10^{-19}}{9.1 \times 10^{-31}}$

$= 7.25 \times 10^{10}$

or $v_2 = \mathbf{2.7 \times 10^5\ ms^{-1}}.$

Problem 5. *In a full wave junction diode rectifier, the input a.c. has an rms value of 10 V. The transformer used is a step up transformer having transformation ratio 1 : 2. Calculate the d.c. and a.c. voltages in the rectified output.*

Solution. rms value of input a.c., $V_{rms} = 10$ V

Peak value of input a.c.,

$V_0 = \sqrt{2}\ V_{rms} = \sqrt{2} \times 10 = 14.14$ V

As the step-up transformer has transformation ratio 1 : 2, the maximum value of the output voltage of the transformer applied to the diodes is

$$V_0' = 2 \times V_0 = 2 \times 14.14 = 28.28 \text{ V}$$

d.c. voltage in the rectified output $= \dfrac{2\,V_0'}{\pi}$

$$= 0.637 \times 28.28 = \mathbf{18.01\ V.}$$

a.c. voltage in the rectified output

$$= 0.305\ V_0' = 0.305 \times 28.28 = \mathbf{8.62\ V.}$$

Problem 6. *The transfer characteristic of a base-biased transistor in CE configuration is as shown in Fig. 14.194. Name the region corresponding to the values (i) 0 to V_1 to V_2 (iii) greater than V_2 of the input voltage applied to the transistor.*

Identify the voltage range that should not be used if the transistor has to work as a switch. What is the practical use of transistor, when it is operated in this voltage range ? Name the source that results in a higher energy of the output of a transistor operated in this range. **[CBSE Sample Paper 11]**

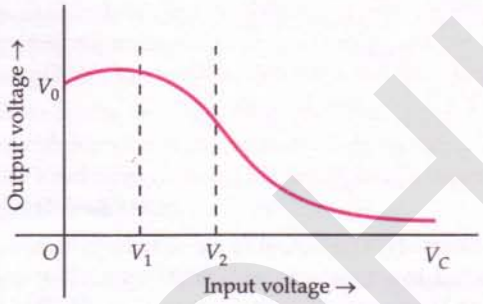


Fig. 14.194

Solution. (*i*) 0 to V_1 = Cut off region

(*ii*) V_1 to V_2 = Active region

(*iii*) Grater than V_2 = Saturation region

For the transistor to work as a switch, it should not be used in the active region *i.e.*, from V_1 to V_2.

The energy for the higher a.c. power at the output is supplied by the biasing battery.

Problem 7. *An n-p-n transistor in a common-emitter mode is used as a simple voltage-amplifier with a collector-current of 4 mA. The terminal of a 8-V battery is connected to the collector through a load-resistance R_L and to the base through a resistance R_B. The collector-emitter voltage $V_{CE} = 4$ V, the base-emitter voltage $V_{BE} = 0.6$ V and the current amplification factor $\beta_{dc} = 100$. Calculate the values of R_L and R_B.* **[Roorkee 97]**

Solution. An *n-p-n* transistor in a common-emitter mode with connections as given is shown in Fig. 14.195.

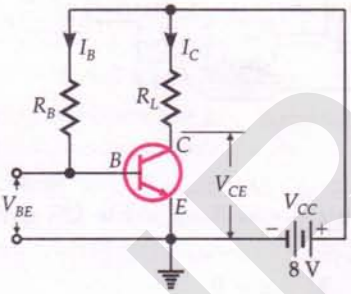


Fig. 14.195

Collector emitter voltage,

$$V_{CE} = V_{CC} - I_C R_L$$

$$\therefore \quad R_L = \frac{V_{CC} - V_{CE}}{I_C}$$

$$= \frac{8\text{ V} - 4\text{ V}}{4 \times 10^{-3}\text{ A}}$$

$$= 10^3\ \Omega = 1\ \text{k}\Omega$$

As $\beta_{dc} = \dfrac{I_C}{I_B}$

$$\therefore \quad I_B = \frac{I_C}{\beta_{dc}} = \frac{4 \times 10^{-3}\text{ A}}{100} = 4 \times 10^{-5}\text{ A}$$

Base-emitter voltage,

$$V_{BE} = V_{CC} - I_B R_B$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{8\text{ V} - 0.6\text{ V}}{4 \times 10^{-5}\text{ A}}$$

$$= 1.85 \times 10^5\ \Omega = \mathbf{185\ k\Omega.}$$

Problem 8. *Write the truth table for the circuit shown in Fig. 14.196. Show that it represents a XOR gate.*

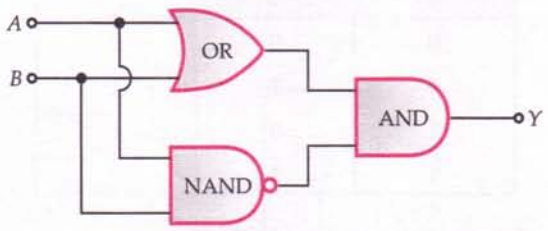


Fig. 14.196

Solution. (*a*) The given circuit contains an OR, a NAND and an AND gate, as shown in Fig. 14.197.

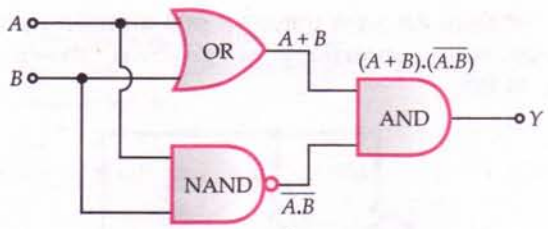


Fig. 14.197

The inputs A and B are fed to OR gate so that its output is

$$Y' = A + B$$

Also, the inputs A and B are fed to NAND gate so that its output is

$$Y'' = \overline{A.B}$$

Then Y and Y'' are fed to AND gate so that the output is

$$Y = Y'.Y'' = (A + B).(\overline{A.B})$$

The logic table for the given circuit is

OR gate			NAND gate			AND gate		
Inputs		Output	Inputs		Output	Inputs		Output
A	B	$Y'=A+B$	A	B	$Y''=\overline{A.B}$	Y'	Y''	$Y=Y'.Y''$
0	0	0	0	0	1	0	1	0
0	1	1	0	1	1	1	1	1
1	0	1	1	0	1	1	1	1
1	1	1	1	1	0	1	0	0

Hence the truth table for the given circuit is

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

which is the truth table of XOR gate.

Problem 9. *Input signals A and B are applied to the input terminals of the 'dotted box' set-up shown here. Let Y be the final output signal from the box.*

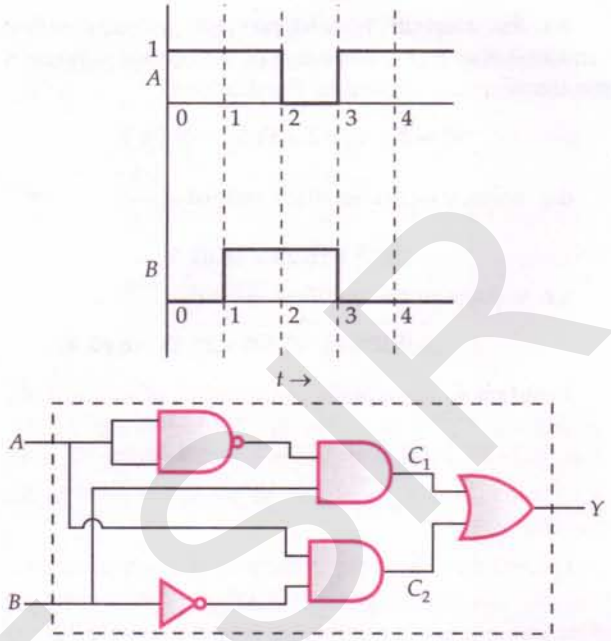


Fig. 14.198

Draw the waveforms of the signals labelled as C_1 and C_2 within the box, giving (in brief) the reasons for getting these waveforms. Hence draw the waveform of the final output signal Y. Give reasons for your choice.

What can we state (in words) as the relation between the final output signal Y and the input signals A and B ?

[CBSE Sample Paper 08]

Solution. (*i*) The NAND gate with both its terminals connected together acts as a NOT gate. The input A given to it appears $\overline{A}$ as its output [Fig. 14.199(*c*)].

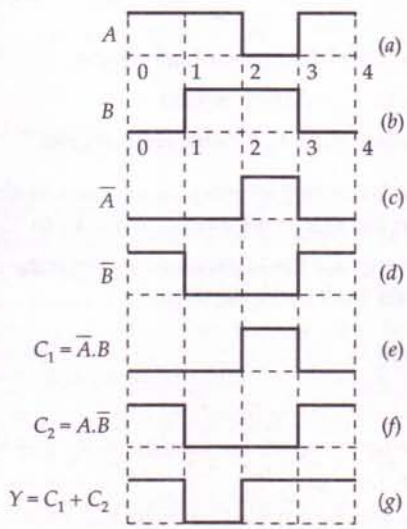


Fig. 14.199

(*ii*) The input B given to the NOT get appears $\overline{B}$ as the output [Fig. 14.199(*d*)].

(*iii*) For the upper AND gate, $\overline{A}$ and B are the inputs. Its output is

$$C_1 = \overline{A} \,.\, B$$

The waveform of C_1 is shown in Fig. 14.199(*e*).

(*iv*) For the lower AND gate, the inputs are A and $\overline{B}$.

Its output is $C_2 = A \,.\, \overline{B}$

The waveform of C_2 is shown in Fig. 14.199(*f*).

(*v*) For the last OR gate, C_1 and C_2 are the inputs. Its output is

$$Y = C_1 + C_2$$

The waveform of Y is shown in Fig. 14.199(*g*).

On comparing the output Y with the inputs A and B, we conclude that

(*i*) The output Y is low (0) when both the inputs A and B are high (1).

(*ii*) The output Y is high (1) when either of the inputs A or B is low and the other is high.

14.1 *In an n-type silicon, which of the following statement is true :*

(a) *Electrons are majority carriers and trivalent atoms are the dopants.*

(b) *Electrons are minority carriers and pentavalent atoms are the dopants.*

(c) *Holes are minority carriers and pentavalent atoms are the dopants.*

(d) *Holes are majority carriers and trivalent atoms are the dopants.*

Ans. (c) In an *n*-type silicon, holes are minority carriers and pentavalent atoms are the dopants.

14.2. *Which of the statements given in Exercise 14.1 is true for p-type semiconductors ?*

Ans. (d) In a *p*-type semiconductor, holes are majority carriers and trivalent atoms are the dopants.

14.3. *Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands separated by energy band gap respectively equal to* $(E_g)_C$, $(E_g)_{Si}$ *and* $(E_g)_{Ge}$. *Which of the following statements is true ?* **[AIIMS 13]**

(a) $(E_g)_{Si} < (E_g)_{Ge} < (E_g)_C$.

(b) $(E_g)_C < (E_g)_{Ge} > (E_g)_{Si}$.

(c) $(E_g)_C > (E_g)_{Si} > (E_g)_{Ge}$.

(d) $(E_g)_C = (E_g)_{Si} = (E_g)_{Ge}$.

Ans. (c) The energy band gap is largest for carbon, less for silicon and least for germanium.

14.4. *In an unbiased p-n junction, holes diffuse from the p-region to n-region because*

(a) *free electrons in the n-region attract them.*

(b) *they move across the junction by the potential difference.*

(c) *hole concentration in p-type region is more as compared to n-region.*

(d) *All the above.*

Ans. (c) In an unbiased *p-n* junction, holes diffuse from the *p*-region to *n*-region because hole concentration in *p*-region is more as compared to *n*-region.

14.5. *When a forward bias is applied to a p-n junction, it*

(a) *raises the potential barrier.*

(b) *reduces the majority carrier current to zero.*

(c) *lowers the potential barrier.*

(d) *none of the above.*

Ans. (c) When a forward bias is applied to a *p-n* junction, it opposes the potential barrier and hence lowers it.

14.6. *For transistor action, which of the following statements are correct :*

(a) *Base, emitter and collector regions should have similar size and doping concentrations.*

(b) *The base region must be very thin and lightly doped.*

(c) *The emitter junction is forward biased and collector junction is reverse biased.*

(d) *Both the emitter junction as well as the collector junction are forward biased.*

Ans. (b) and (c) are correct.

14.7. *For a transistor amplifier, the voltage gain*

(a) *remains constant for all frequencies.*

(b) *is high at high and low frequencies and constant in the middle frequency range.*

(c) *is low at high and low frequencies and constant at mid frequencies.*

(d) *none of the above.*

Ans. (c) The voltage gain is low at high and low frequencies and constant in the middle frequency range.

14.8. *In half-wave rectification, what is the output frequency if the input frequency is 50 Hz. What is the output frequency of a full-wave rectifier for the same input frequency ?*

Ans. Input frequency = 50 Hz

In half-wave rectification, only one ripple is obtained per cycle of the output.

∴ Output frequency of a half-wave rectifier

= Input frequency = **50 Hz**

In full wave rectification, two ripples are obtained per cycle of the output.

∴ Output frequency of full wave rectifier

= 2 × Input frequency = 2 × 50 = **100 Hz.**

14.9. *For a CE-transistor amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 2 V. Suppose the current amplification factor of the transistor is 100, find the input signal voltage and base current, if the base resistance is 1 kΩ.*

Ans. Here $R_C = 2\,k\Omega = 2000\,\Omega$, $R_B = 1\,k\Omega = 1000\,\Omega$, $\beta = 100$, $V_0 = 2$ V

(*i*) Voltage gain,

$$\frac{V_0}{V_i} = \frac{\beta R_0}{R_i}$$

or $$\frac{2}{V_i} = 100 \times \frac{2000}{1000}$$

∴ Input signal voltage, $V_i = \mathbf{0.01\ V}$.

(*ii*) $\beta = \dfrac{I_C}{I_B} = \dfrac{V_0 / R_C}{I_B}$.

∴ Base current,

$$I_B = \frac{V_0}{\beta R_C} = \frac{2}{100 \times 2000} = 10^{-5}\,\text{A} = \mathbf{10\ \mu A}.$$

14.10. *Two amplifiers are connected one after the other in series (cascaded). The first amplifier has a voltage gain of 10 and the second has a voltage gain of 20. If the input signal is 0.01 V, calculate the output a.c. signal.*

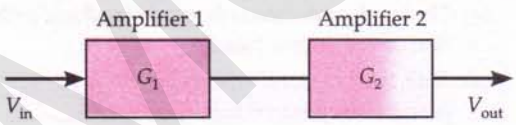


Fig. 14.200

Ans. Here $G_1 = 10$, $G_2 = 20$, $V_i = 0.01$ V, $V_o = ?$

Total gain, $G = G_1 G_2$

or $$\frac{V_o}{V_i} = G_1 G_2$$

∴ $$V_o = G_1 G_2 V_i$$

$$= 10 \times 20 \times 0.01 = \mathbf{2\ V}.$$

14.11. *A p-n photodiode is fabricated from a semiconductor with a band gap of 2.8 eV. Can it detect a wavelength of 6000 nm ?* [CBSE D 05]

Ans. Energy required to cross the band gap,

$$E_g = 2.8\,\text{eV}$$

Wavelength of incident photon,

$$\lambda = 6000\,\text{nm} = 6 \times 10^{-6}\,\text{m}$$

Energy of incident photon,

$$E = \frac{hc}{\lambda}$$

$$= \frac{6.63 \times 10^{-34} \times 3 \times 10^8}{6 \times 10^{-6}} = 0.207\,\text{eV}$$

As $E < E_g$, the *p-n* junction **cannot detect** the radiation of wavelength 6000 nm.

14.12. *The number of silicon atoms per m^3 is 5×10^{28}. This is doped simultaneously with 5×10^{22} atoms per m^3 of Arsenic and 5×10^{20} per m^3 atoms of Indium. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16}\,m^{-3}$. Is the material n-type or p-type ?*

Ans. Here $N_D = 5 \times 10^{22}\,\text{m}^{-3}$,

$N_A = 5 \times 10^{20}\,\text{m}^{-3}$, $n_i = 1.5 \times 10^{16}\,\text{m}^{-3}$.

For the semiconductor to remain electrically neutral,

$$N_D - N_A = n_e - n_h \qquad ...(1)$$

Also $$n_e\, n_h = n_i^2$$

∴ $$(n_e + n_h)^2 = (n_e - n_h)^2 + 2n_e\, n_h$$

$$= (N_D - N_A)^2 + 4n_i^2 \qquad ...(2)$$

$$n_e + n_h = \sqrt{(N_D - N_A)^2 + 4n_i^2}$$

Adding equations (1) and (2), we get

$$n_e = \frac{1}{2}(N_D - N_A) + \sqrt{(N_D - N_A)^2 + 4n_i^2}$$

$$= \frac{1}{2}[(5 \times 10^{22} - 0.05 \times 10^{22}) + \sqrt{(4.95 \times 10^{22})^2 + 4 \times (1.5 \times 10^{16})^2}]$$

$$\approx \frac{1}{2}[4.95 \times 10^{22} + \sqrt{(4.95 \times 10^{22})^2}]$$

$$= \mathbf{4.95 \times 10^{22}\ m^{-3}}$$

$$n_h = \frac{n_i^2}{n_e}$$

$$= \frac{(1.5 \times 10^{16})^2}{4.95 \times 10^{22}} = \frac{2.25 \times 10^{32}}{4.95 \times 10^{22}}$$

$$= \mathbf{4.5 \times 10^9\ m^{-3}}.$$

As $n_e > n_h$, the material is of ***n-type***.

14.13. *In an intrinsic semiconductor, the energy gap E_g is 1.2 eV. Its hole mobility is very much smaller than electron mobility and is independent of temperature. What is the ratio between conductivity at 600 K and that at 300 K? Assume that the temperature dependence of intrinsic carrier concentration n_i is expressed as*

$$n_i = n_0 \exp\left[\frac{-E_g}{2k_B T}\right]$$

where n_0 is a constant and $k_B = 8.62 \times 10^{-5}$ eVK^{-1} is the Boltzmann constant.

Ans. As $\mu_e >> \mu_h$, and for an intrinsic semiconductor

$$n_e = n_h = n_i$$

$\therefore$ Conductivity is given by

$$\sigma = e(n_e\mu_e + n_h\mu_h)$$

$$= en_i(\mu_e + \mu_h) \simeq en_i\mu_e \qquad [\because \mu_e >> \mu_h]$$

But $$n_i = n_0 \exp\left[\frac{-E_g}{2k_B T}\right]$$

$\therefore$ $$\sigma = e\mu_e n_0 \exp\left[\frac{-E_g}{2k_B T}\right]$$

Here all the pre-exponential terms are assumed independent of temperature. So we can put a constant

$$\sigma_0 = e\mu_e n_0$$

and express the conductivity as

$$\sigma = \sigma_0 \exp\left[\frac{-E_g}{2k_B T}\right]$$

Now $\frac{E_g}{2} = \frac{1.2}{2} = 0.6$ eV, $k_B = 8.62 \times 10^{-5}$ eVK^{-1}

$\therefore$ $$\sigma(600\text{ K}) = \sigma_0 \exp\left[\frac{-0.6}{8.62 \times 10^{-5} \times 600}\right]$$

$$\sigma(300\text{ K}) = \sigma_0 \exp\left[\frac{-0.6}{8.62 \times 10^{-5} \times 300}\right]$$

Hence

$$\frac{\sigma(600\text{ K})}{\sigma(300\text{ K})} = \frac{\exp\left[\frac{-0.6}{8.62 \times 10^{-5} \times 600}\right]}{\exp\left[\frac{-0.6}{8.62 \times 10^{-5} \times 300}\right]}$$

$$= \exp\left[\frac{0.6}{8.62 \times 10^{-5}}\left(\frac{1}{300} - \frac{1}{600}\right)\right]$$

$$= \exp\left[\frac{0.6 \times 10^5}{8.62 \times 600}\right]$$

$$= \exp(11.6) = 1 \times 10^5.$$

This shows that the conductivity of a semiconductor increases rapidly with the rise in temperature.

14.14. *In a p-n junction diode, the current I can be expressed as $I = I_0 \exp\left(\frac{eV}{2k_B T} - 1\right)$, where I_0 is called the reverse saturation current, V is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, k_B is the Boltzmann constant (8.6×10^{-5} eV/K) and T is the absolute temperature. If for a given diode $I_0 = 5 \times 10^{-12}$ A and T = 300 K, then :*

(a) What will be the forward current at a forward voltage of 0.6 V ?

(b) What will be the increase in the current if the voltage across the diode is increased to 0.7 V ?

(c) What is the dynamic resistance ?

(d) What will be the current if reverse bias voltage changes from 1 V to 2 V ?

Ans. The current I through a junction diode is given as

$$I = I_0\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right]$$

where $I_0 = 5 \times 10^{-12}$ A, $T = 300$ K,

$k_B = 8.6 \times 10^{-5}$ eVK^{-1}

$= 8.6 \times 10^{-5} \times 1.6 \times 10^{-19}$ JK^{-1}.

(*a*) When $V = 0.6$ V

$$\frac{eV}{k_B T} = \frac{1.6 \times 10^{-19} \times 0.6}{8.6 \times 1.6 \times 10^{-24} \times 300}$$

$$= \frac{600}{8.6 \times 3} = 23.26$$

$\therefore$ $$I = I_0\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right]$$

$$= 5 \times 10^{-12}\,[\exp(23.26) - 1]\text{ A}$$

$$= 5 \times 10^{-12}\,[1.2586 \times 10^{10} - 1]\text{ A}$$

$$= 5 \times 10^{-12} \times 1.2586 \times 10^{10}\text{ A}$$

$$= 0.06293\text{ A}.$$

(*b*) When $V = 0.7$ V,

$$\frac{eV}{k_B T} = \frac{1.6 \times 10^{-19} \times 0.7}{8.6 \times 1.6 \times 10^{-24}} = 27.13$$

$\therefore$ $$I = I_0\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right]$$

$$= 5 \times 10^{-12}\,[\exp(27.13) - 1]\text{ A}$$

$$= 5 \times 10^{-12}\,[6.07 \times 10^{11} - 1]\text{ A}$$

$$\simeq 5 \times 10^{-12} \times 6.07 \times 10^{11}\text{ A} = 3.035\text{ A}$$

Increase in current,

$$\Delta I = 3.035 - 0.06293 = \mathbf{2.972\text{ A}}.$$

(*c*) For $\Delta V = 0.7 - 0.6 = 0.1$ V, $\Delta I = 2.972$ A

Dynamic resistance,

$$r_d = \frac{\Delta V}{\Delta I} = \frac{0.1}{2.972} = 0.0336\,\Omega.$$

(*d*) For both the voltages, the current I will be almost equal to I_0, showing almost infinite dynamic resistance in the reverse bias.

$$I \simeq -I_0 = -5 \times 10^{-12}\ \text{A}.$$

14.15. *You are given the two circuits as shown in Fig. 14.201. Show that the circuit (a) acts as OR gate while the circuit (b) acts as AND gate.* [CBSE OD 11]

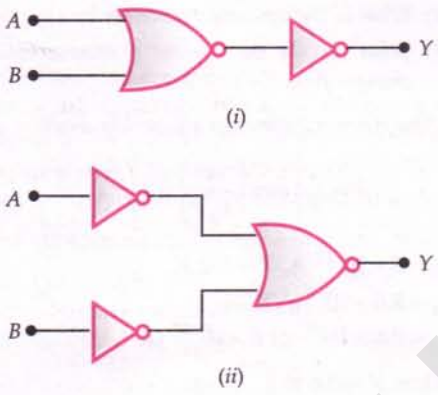


Fig. 14.201

Ans. Refer to the solution of Example 50 on page 14.60.

14.16. *You are given two circuits as shown in Fig. 14.202, which consist of NAND gates. Identify the logic operation carried out by the two circuits.* [CBSE D 09C, 11 ; OD 11]

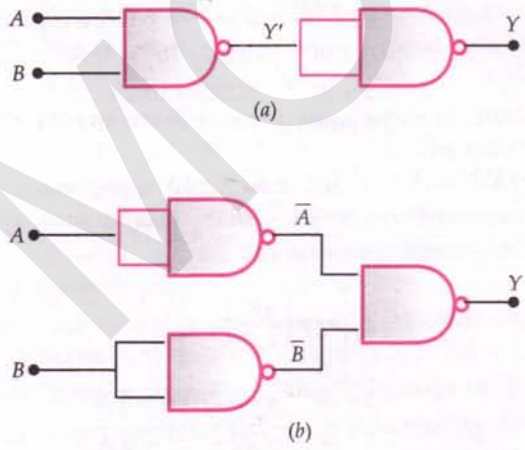


Fig. 14.202

Ans. Refer to the solution of Example 52 on page 14.60.

14.17. *Write the truth table for a NAND gate connected as given in Fig. 14.203. Hence identify the exact logic operation carried out by this circuit.*

Ans. Refer to the solution of Example 51 on page 14.60.

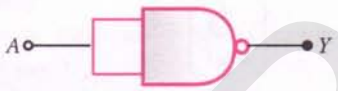


Fig. 14.203

14.18. *Write the truth table for circuit given in Fig. 1[illegible] below consisting of NOR gates and identify the logic ope[illegible] (OR, AND, NOT) which this circuit is performing.*

Ans. Refer to the solution of Example 48 on page 14.59.

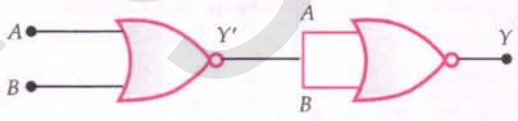


Fig. 14.204

14.19. *Write the truth table for circuit given in Fig. 14.205 consisting of NOR gates only. Identify the logic operations (OR, AND, NOT) performed by the two circuits.* [CBSE D 09C]

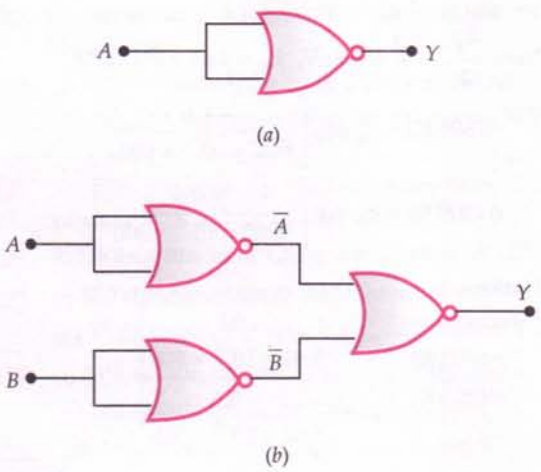


Fig. 14.205

Ans. Refer to the solution of Example 49 on page 14.59.

Text Based Exercises

TYPE A : VERY SHORT ANSWER QUESTIONS (1 mark each)

1. What is an energy band in a solid ? [ISCE 2000]
2. What is valence band ?
3. What is conduction band ?
4. Define forbidden energy gap in solids. [Punjab 04]
5. What is Fermi energy level ? [Punjab 02, 04]
6. How much is the energy gap in a conductor ?
7. What is the order of energy gap in a semiconductor ? [CBSE D 96C]
8. What is the order of energy gap in an insulator ?
9. Name the charge carriers in the following at room temperature :
   (*i*) Conductor (*ii*) Intrinsic semiconductor
   (*iii*) Insulator [ISCE 97]
10. At what temperature would an intrinsic semiconductor behave like a perfect insulator ? [CBSE D 08C]
11. What is an intrinsic semiconductor ? [Haryana 93]
12. Give the ratio of the number of holes and number of conduction electrons, in an intrinsic semiconductor.
13. What is doping ? [Himachal 97, 01]
14. What is an extrinsic or a doped semiconductor ? [Punjab 02, 03]
15. What is an *n*-type semiconductor ?
16. What is a *p*-type semiconductor ? [ISCE 01]
17. Doping silicon with indium leads to which type of semiconductor ?
18. What elements other than indium and gallium can be used to form a *p*-type semiconductor ?
19. What type of charge carriers are there in a *p*-type semiconductor ? [CBSE D 98]
20. Name any one element, other than 'As' and 'Sb', which can be used as impurity with germanium to form *n*-type semiconductor. [CBSE OD 96]
21. Is the ratio of number of holes and number of electrons in an *n*–type extrinsic semiconductor more than, less than or equal to 1 ? [CBSE D 97]
22. What type of charge carriers are there in an *n*-type semiconductor ? [CBSE D 97 ; Haryana 04]
23. What type of impurity is added to obtain *n*-type semiconductor ? [Himachal 99C]
24. What are donor impurity atoms ?
25. What are acceptor impurity atoms ?
26. The forbidden energy gaps in insulators, semiconductors and conductors are EG_1, EG_2 and EG_3 respectively. Arrange them in ascending order.
27. A semiconductor has equal electron and hole concentration of $6 \times 10^4 m^{-3}$. On doping with a certain impurity, electron concentration increases to $8 \times 10^{12} m^{-3}$. Identify the type of the semiconductor. [CBSE D 04]
28. How does the energy gap of an intrinsic semiconductor vary, when doped with a trivalent impurity ? [CBSE D 2000]
29. What are the majority charge carriers in a *p*-type semiconductor ? [Roorkee 96]
30. Is there any hole in an *n*-type semiconductor ?
31. What is the distinction between a pure semiconductor and a semiconductor made from metals ?
32. Define mobility of a charge carrier. Give its unit.
33. Which has a higher mobility–electron or hole ?
34. Is Ohm's law obeyed by semiconductors ?
35. What is a junction diode ? Give its pictorial symbol.
36. What is depletion region in a *p*-*n* junction ? [CBSE D 92 ; ISCE 97]
37. Which process causes depletion region in a *p*-*n* junction ? [CBSE D 92]
38. What is the thickness of depletion layer in a *p*-*n* junction ?
39. Name the type of biasing of a *p*-*n* junction diode so that the junction offers very high resistance. [CBSE D 05C]
40. What happens when a forward bias is applied to *p*-*n* junction ? [CBSE OD 15]
41. How does the width of the depletion region of a *p*-*n* junction vary, if the reverse bias applied to it decreases ? [CBSE OD 02, 08]
42. Give an approximate value for the potential barrier of a silicon type junction diode.
43. Under what condition does a *p*-*n* junction work as an open switch ?
44. What is an ideal junction diode ?
45. What is zener breakdown ?
46. Define resistance of a junction diode. [CBSE D 93]
47. The resistance of a *p*-*n* junction is of the order of a few ohm. Is the *p*-*n* junction forward or reverse biased ?

48. How much is the resistance of a *p-n* junction when it is reverse biased ?
49. In Fig. 14.206, is the diode *D* forward or reverse biased ? [CBSE D 97]

Fig. 14.206

50. What is the order of reverse current in a reverse biased *p-n* junction ?
51. A junction diode has an avalanche breakdown. Is it heavily or lightly doped ?
52. What is the order of breakdown voltage in an avalanche zener diode ?
53. Draw energy band diagram for an intrinsic semiconductor. [CBSE OD 98]
54. Draw energy-band diagram for an *n*-type extrinsic semiconductor. [CBSE OD 98, 02]
55. Draw energy-band diagram for a *p*-type extrinsic semiconductor. [CBSE OD, 98, 01]
56. Draw the voltage-current characteristic of a *p-n* junction diode in forward bias. [CBSE OD 04]
57. Draw the voltage-current characteristic of a zener diode. [CBSE OD 04]
58. Draw a *p-n* junction with reverse bias. [Punjab 03]
59. State the function of a Zener diode in a circuit. [ISCE 93]
60. Draw the V-I characteristic of a *p-n* junction. Show the zener voltage on the characteristic curve.
61. What is a transistor ?
62. What is the full form of transistor ? [Himachal 04]
63. In an *n-p-n* transistor, what are the current carriers inside and outside the transistor circuit ?
64. In a *p-n-p* transistor, what are the current carriers inside and outside the transistor circuit ?
65. Is transistor a current controlled or temperature controlled device ?
66. What kinds of biasing are required to the collector and base of a transistor in a common emitter amplifier ? [ISCE 98]
67. What is the relation between emitter current I_E, base current I_B, and collector current I_C at any instant in a properly biased common emitter transistor circuit ? Which one of the three has smallest magnitude ? [ISCE 98]
68. In the normal operation of a transistor, what is the order of magnitude of currents, I_E, I_C and I_B ?
69. Name the parameters of a transistor.
70. Define voltage gain of an amplifier.
71. Define the transconductance of a transistor. On what factors does it depend ? [CBSE D 96 ; OD 93C]
72. Define current gain for a transistor. [ISCE 02]

Or

Define current amplification factor in a common emitter mode of transistor. [Haryana 94, 04]

73. Define a.c. voltage gain of common emitter transistor amplifier.
74. Define the input resistance for the common emitter transistor.
75. Define the output resistance of common emitter transistor.
76. What is relation between power gain, current gain and resistance gain of a transistor amplifier ?
77. What is relation between power gain, voltage gain and current gain of a transistance amplifier ?
78. What is relation between voltage gain and transconductance of a transistor amplifier ?
79. A transistor is being used as a common emitter amplifier. What is the value of phase difference, if any, between the collector-emitter voltage and input signal ? [CBSE Sample Paper 1997]
80. In a transistor, doping level in base is increased slightly. How will it affect (*i*) collector current and (*ii*) base current ? [CBSE D 11]
81. How does the collector current change in a junction transistor, if the base region has larger width ? [CBSE D 99]
82. Write the relation between current gains α or β. [Haryana 04]
83. Calculate the current gain β of a transistor, if the current gain $\alpha = 0.98$. [ISCE 95]
84. For a transistor the value of β is 100, what is the value of α ?
85. What is an oscillator ?
86. What is a basic oscillator circuit ?
87. Do the oscillations of a tank circuit have a constant amplitude ?
88. What is feedback ?
89. What is positive feedback ?
90. What is the type of feedback required in an oscillator ? [CBSE D 96C]
91. State two disadvantages of semiconductor devices. [Punjab 03]
92. Name the two types of electronic circuits.
93. What is analog signal ? [CBSE D 12]
94. What is a digital signal ? [CBSE D 12]
95. Give some examples of analog electronic devices.

96. Give some examples of digital electronic devices.
97. What is a logic gate ? [Haryana 97C ; Punjab 04]
98. What is a Boolean expression ?
99. What do you mean by truth table of a logic gate ?
100. What are the three basic logic gates ?
101. What is an OR gate ? Give Boolean expression for it.
102. Draw the logic symbol of an OR gate. [Himachal 02 ; Haryana 04]
103. Write the truth table of an OR gate. [CBSE OD 95 ; Haryana 02]
104. What is an AND gate ? Give its Boolean expression.
105. Draw the logic symbol of AND gate. [Himachal 02 ; CBSE OD 09, 14C]
106. Write the truth of AND gate. [CBSE OD 09, 14C ; Haryana 02]
107. What is a NOT gate ? Give Boolean expression for it.
108. Draw the logic symbol of NOT gate. [Himachal 02]
109. Write the truth table for NOT gate. [Haryana 02 ; CBSE OD 13C]
110. Give the logic symbol of NAND gate. [CBSE OD 15C]
111. Write the truth table for NAND gate. [CBSE OD 13C, 15C]
112. Give the logic symbol of a NOR gate. [CBSE OD 09]
113. Write the truth table for a NOR gate. [CBSE F 95 ; Haryana 02]
114. Write the truth table for the combination of gates shown in Fig. 14.207. [CBSE D 97 ; Haryana 2000]

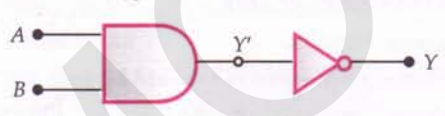


Fig. 14.207

115. When is the output of an OR gate high ?
116. When is the output of a NAND gate low ?
117. Which gate is equivalent to a NAND gate having both its inputs A and B connected together ?
118. How can a NAND gate be used as an invertor ?
119. How many NAND gates are required to realise (*i*) a NOT gate and (*ii*) an AND gate ?
120. How many NAND gates are required to realise an OR gate ?
121. What is an integrated circuit ?
122. Write the full form of the terms (*i*) SSI and (*ii*) VLSI used for different types of integrated circuits. [CBSE OD 04C]
123. Write the full forms of the terms (*i*) MSI and (*ii*) LSI used for different types of integrated circuits. [CBSE D 04C]
124. Zener diodes have higher dopant densities as compared to ordinary $p-n$ junction diodes. How does it affect the
(*i*) Width of the depletion layer ?
(*ii*) Junction field ? [CBSE Sample Paper 08]
125. State the factor, which controls :
(*i*) wavelength of light, and
(*ii*) intensity of light
emitted by an LED [CBSE OD 08 ; F 08]
126. Visible light photons are known to have energies ranging (nearly) 1.8 eV to 2.8 eV. Use this information to reason out why silicon is not a suitable semiconductor for designing visible light LEDs ? [CBSE OD 07C]
127. How is the band gap 'E_g' of a photodiode related to the maximum wavelength λ_m, that can be detected by it ? [CBSE Sample Paper 08]
128. Why should a photodiode be operated at a reverse bias ? [CBSE OD 08]
129. State the reason, why GaAs is most commonly used in making of a solar cell. [CBSE OD 08]
130. What is the function of a photodiode ? [CBSE OD 13C]
131. An unknown input (A) and the input (B) shown here, are used as the two inputs in a NAND gate. The output Y, has the form shown below. Identify the intervals over which the input 'A' must be 'low'. [CBSE Sample Paper 08]

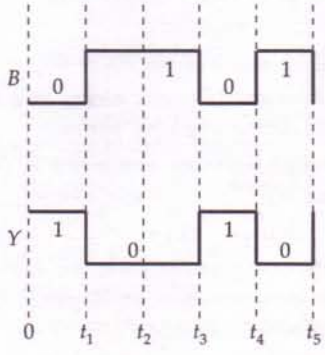


Fig. 14.208

Answers

1. A very large number of energy levels lying closely within a small energy range of a solid form an energy band.
2. The highest energy band filled with valence electrons is called valence band.
3. The lowest unfilled allowed energy band next to valence band is called conduction band. Current conduction is due to the electrons in this band.
4. The energy gap between the valence band and the conduction band in which no allowed energy levels can exist is called forbidden energy gap.
5. Refer to point 7 of Glimpses on page 14.107.
6. Zero. 7. 1 eV.
8. 6 eV for an insulator like diamond.
9. (*i*) Electrons (*ii*) Electrons and holes (*iii*) None.
10. At 0 K.
11. Refer to point 9 of Glimpses on page 14.108.
12. In an intrinsic semiconductor,
    $n_h = n_e = n_i$, therefore, $n_h : n_e = \mathbf{1:1}$.
13. Refer to point 10 of Glimpses on page 14.108.
14. Refer to point 11 of Glimpses on page 14.108.
15. A tetravalent semiconductor of Si or Ge doped with pentavalent impurity atoms of As, Sb or P is called an *n*-type semiconductor.
16. A tetravalent semiconductor of Si or Ge doped with trivalent impurity atoms of B, Al or In is called a *p*-type semiconductor
17. *p*-type semiconductor.
18. Boron (B) or aluminium (Al).
19. Holes as majority charge carriers and electrons as minority charge carriers.
20. Phosphorous (P).
21. Less than 1.
22. Electrons as majority charge carriers and holes as minority charge carriers.
23. Pentavalent atoms of Sb, As or P.
24. The pentavalent impurity atoms like As, P and Sb are called donor impurity atoms.
25. The trivalent impurity atoms like B, Al, Ga and In are called acceptor impurity atoms.
26. $EG_3 < EG_2 < EG_1$.
27. As the electron concentration becomes greater than the hole concentration on doping, the resulting semiconductor is of *n*-type.
28. The energy gap in the semiconductor decreases due to the creation of acceptor energy level just above the top of the valence band.
29. Holes.
30. Yes. In *n*-type semiconductors, holes are formed due to breaking of covalent bonds. But they are minority charge carriers.
31. The resistance of a pure semiconductor (*e.g.*, Ge and Si) decreases with the increase in temperature. But the resistance of a semiconductor made from metals increases with the increase in temperature.
32. Refer to point 15 of Glimpses on page 14.108.
33. An electron has a higher mobility than a hole in a semiconductor.
34. In semiconductors, Ohm's law is obeyed only for low electric fields ($E < 10^6$ Vm^{-1}). Above this field, the current becomes independent of the applied voltage.
35. A junction diode or a *p*-*n* junction is a single crystal of Ge or Si doped in such a manner that one half portion of it is *p*-type semiconductor and other half portion is *n*-type semiconductor. Its circuit symbol is shown in Fig. 14.209.

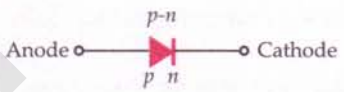


Fig. 14.209 Symbol of junction diode.

36. It is a thin region around the junction of *p* - and *n*-sections which is devoid of free electrons and holes and has immobile ions only.
37. The diffusion of electrons and holes across the *p*-*n* junction causes the depletion region.
38. About 1 μm ($= 10^{-6}$ m).
39. Reverse biasing.
40. When a *p*-*n* junction is forward biased,
    (*i*) the potential barrier across the junction decreases,
    (*ii*) the width of the depletion layer decreases,
    (*iii*) the effective resistance across the junction decreases,
    (*iv*) the junction conducts current.
41. If the reverse bias decreases, the width of depletion region of the *p*-*n* junction increases.
42. 0. 7 V.
43. When the *p*-*n* junction is reverse biased.
44. A junction diode which conducts when forward biased and does not conduct when reverse biased is called an ideal junction diode. It offers zero resistance in forward biasing and infinite resistance in reverse biasing.

45. When a large reverse voltage is applied across a *p-n* junction, a large reverse current flows through it. This effect is called zener breakdown.
46. Refer to point 19 of Glimpses on page 14.109.
47. Forward biased.
48. Very high of the order of few k Ω.
49. The diode *D* is reverse biased because its *p*-side is at lower potential.
50. It is of the order of few μA.
51. Lightly doped.
52. 200 V.
53. See Fig. 14.11(*a*) (*ii*).
54. See Fig. 14.11(*b*).
55. See Fig. 14.11(*c*).
56. See Fig. 14.18.
57. See Fig. 14.29.
58. See Fig. 14.16(*a*).
59. A Zener diode can be used as a voltage regulator.
60. See Fig. 14.29.
61. Refer to point 27 of Glimpses on page 109.
62. The word *transistor* is short form of *transference* of signal across a *resistor*.
63. Electrons are current carriers through the *n-p-n* transistor and in the external circuit.
64. Holes are the current carriers through the *p-n-p* transistor but in the external circuit current is carried by electrons.
65. Transistor is a current controlled device.
66. The base emitter junction is forward biased while the collector-emitter junction is reverse biased.
67. $I_E = I_B + I_C$. The base current I_B has the smallest magnitude.
68. I_E and I_C are of the order of mA and I_B is of the order of μA.
69. The parameters of a transistor are
    (*i*) Emitter current (I_E)
    (*ii*) Collector current (I_C)
    (*iii*) Base current (I_B)
    (*iv*) Emitter-base voltage (V_{EB})
    (*v*) Collector-base voltage (V_{CB}).
70. The voltage gain of an amplifier is the ratio of the change in the output voltage (ΔV_0) to the corresponding change in the input voltage (ΔV_i).

    Voltage gain = $A_v = \dfrac{\Delta V_o}{\Delta V_i}$.
71. Refer to point 37(*v*) of Glimpses on page 14.111.
72. The a.c. current gain of *CE* transistor amplifier is defined as the ratio of the small change in the collector current (ΔI_C) to the small change in the base current (ΔI_B), when the collector-emitter voltage is kept constant. It is given by

$$\beta_{ac} \text{ or } A_i = \left[\frac{\Delta I_C}{\Delta I_B}\right]_{V_{CE} = \text{constant}}$$

73. The a.c. voltage gain of *CE* transistor amplifier is defined as the ratio of the small change in output voltage (ΔV_{CE}) to the small change in input voltage (ΔV_{BE}). It is given by

$$A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}}.$$

74. Refer to point 30(*i*) of Glimpses on page 14.110.
75. Refer to point 30(*ii*) of Glimpses on page 14.110.
76. Power gain = (Current gain)^2 × Resistance gain.
77. Power gain = Voltage gain × Current gain.
78. Voltage gain
    = Trans-conductance × Output resistance
79. 180° or π radian.
80. (*i*) Collector current decreases.
    (*ii*) Base current increases.
81. The collector current becomes smaller because of the increase in the rate of recombination of electrons and holes as they move across the emitter base junction.
82. $\beta = \dfrac{\alpha}{1-\alpha}$.
83. $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.98}{1-0.98} = \mathbf{49.}$
84. $\alpha = \dfrac{\beta}{1+\beta} = \dfrac{100}{1+100} = \mathbf{0.99.}$
85. An oscillator is an electronic device that produces electric oscillations of constant frequency and amplitude.
86. The basic oscillatory circuit is the parallel combination of inductance *L* and capacitance *C*. It is called *LC*-or tank circuit.
87. No, the oscillations get damped due to resistive losses in the inductance and dielectric losses in the capacitor.
88. When a part of the output signal is supplied back to the input signal, the process is known as feedback.
89. If feedback signal is in phase with the input signal, it is called positive feedback.
90. Positive feedback.
91. (*i*) Semiconductor devices are very sensitive to the changes of temperature whereas the vacuum tubes are less sensitive.
    (*ii*) Semiconductor devices cannot handle as much power as vacuum tubes.

92. The two types of electronic circuits are (*i*) analog circuits and (*ii*) digital circuits.

93. A signal in the form of continuous time-varying current or voltage is called continuous or analog signal. Fig. 14.210 shows a typical sinusoidal analog signal.

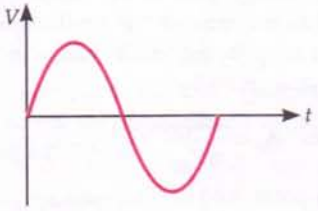


Fig. 14.210

94. A digital signal is a two level voltage signal *e.g.* a signal of 0 V may be used to represent binary 0 and a signal of 5 V to represent binary 1. Digital signals are in the form of pulses of equal level, as shown in Fig. 14.211.

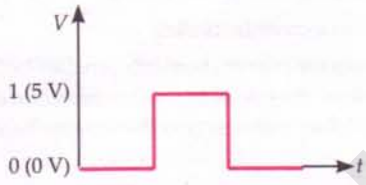


Fig. 14.211

95. Avometer, amplifiers, radio and television are examples of analog devices.

96. Calculators, computers, electronic watches and robots are examples of digital devices.

97. A logic gate is a digital circuit which follows a logical relationship between input and output voltages.

98. It is an equation which describes the functioning of a logic gate. It relates all possible inputs and outputs of a logic gate.

99. It is a table which gives all possible input combinations and the corresponding outputs for a logic gate.

100. The three basic logic gates are : OR, AND and NOT gates.

101. Refer to point 45 of Glimpses on page 14.112.

102. Logic symbol of OR gate is shown in Fig. 14.95.

103. Truth table of OR gate is given in Fig. 14.95.

104. Refer to point 46 of Glimpses on page 14.112.

105. The logic symbol of AND gate is shown in Fig. 14.98.

106. The truth table of AND gate is given in Fig. 14.98.

107. Refer to point 47 of Glimpses on page 14.112.

108. The logic symbol of a NOT gate is shown in Fig. 14.101.

109. Truth table for NOT gate is given in Fig. 14.101.

110. The logic symbol of NAND gate is shown in Fig. 14.105.

111. The truth table for a NAND gate is shown in Fig. 14.105.

112. The logic symbol of a NOR gate is shown in Fig. 14.108.

113. The truth table for a NOR gate is given in Fig. 14.108.

114. The first gate is AND gate and the second is a NOT gate.

The truth table of the combination is as follows :

A	B	$Y' = A.B$	$Y = \overline{A.B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

115. The output of an OR gate is high (1) when any or all of the inputs are high.

116. The output of a NAND gate is low (0) when both the inputs are high (1).

117. It is equivalent to a NOT gate.

118. By connecting together the two inputs of the NAND gate.

119. (*i*) A NOT gate can be made from one NAND gate.
(*ii*) An AND gate can be made from two NAND gates.

120. An OR gate can be realised from three NAND gates.

121. Refer to point 51 of Glimpses on page 14.113.

122. (*i*) SSI stands for small scale integration.
(*ii*) VLSI stands for very large scale integration.

123. (*i*) MSI stands for medium scale integration.
(*ii*) LSI stands for large scale integration.

124. (*i*) Width of the depletion layer is small.
(*ii*) Junction field is high.

125. (*i*) The wavelength of light depends on the nature of the semiconductor used in LED.
(*ii*) Intensity of light depends on the forward bias applied to LED which is controlled by a series resistor R.

126. Si has a band gap of 1.1 eV *i.e.*, its $E_g < 1.8$ eV. So it is not suitable for making visible light LEDs.

127. $E_g = \dfrac{hc}{\lambda_m}$.

128. As fractional change in minority charge carriers is more than the fractional change in majority charge carriers, hence the fractional change due to photo-effects on minority carrier dominated reverse bias current is more easily measurable.

129. GaAs has a better solar conversion efficiency because of its suitable bandgap ($E_g \simeq 1.53$ eV) and high absorption coefficient. So it is a preferred material for solar cells.

130. A photodiode is used to detect optical signals.

131. In intervals 0 to t_1 and t_3 to t_4, the input A may be low.

TYPE B : SHORT ANSWER QUESTIONS (2 or 3 marks each)

1. Give two examples each of
   (*i*) elemental (*ii*) compound inorganic and
   (*iii*) compound organic semiconductors.

2. On the basis of energy band diagrams, distinguish between metals, insulators and semiconductors. [ISCE 94, 98 ; Punjab 10 ; CBSE D 05, OD 05, 10]

3. Draw the energy band diagrams of the following substances :
   (*a*) conductor (*b*) n-type semiconductor
   (*c*) p-type semiconductor
   (*d*) Insulator. [Punjab 99C ; ISCE 2000]

4. Distinguish between extrinsic and intrinsic semiconductors on the basis of energy band diagrams. [CBSE D 15]

5. Distinguish between *n*-type *p*-type semiconductors on the basis of energy band diagrams. [CBSE D 15C]

6. What are the limitations of the intrinsic semiconductors when we use them for developing semiconductor devices ? [Punjab 03]

7. What is doping ? State the necessary conditions for doping. What are the various methods of doping ?

8. Using the concept of electron and hole current, derive an expression for the electrical conductivity of a semiconductor. [Haryana 04 ; Himachal 04]

9. What is an intrinsic semiconductor ? How can this material be converted into (*i*) *p*-type (*ii*) *n*-type extrinsic semiconductor ? Explain with the help of energy band diagrams. [CBSE D 06]

10. How is an *n*-type semiconductor formed ? Name the major charge carriers in it. Draw the energy band diagram of an n-type semiconductor. [CBSE OD 03]

11. How is a *p*-type semiconductor formed ? Name the major charge carriers in it. Draw the energy band diagram of a *p*-type semiconductor. [CBSE OD 03]

12. Draw the energy band diagram of a *p*-type semiconductor. Deduce an expression for the conductivity of a *p*-type semiconductor. [CBSE OD 01]

13. Differentiate between *n*-type and *p*-type semiconductors on the basis of energy band diagrams. Explain the process of conduction in both type of materials. [CBSE Sample Paper 98]

14. What are holes ? Give their important characteristics.

15. Define mobility of a charge carrier. Why is the mobility of an electron in the conduction band of a semiconductor is less than the mobility of a hole (or electron) in the valence band ?

16. Draw the energy band diagram of an *n*-type semiconductor. How does the forbidden energy gap of an intrinsic semiconductor vary with increase in temperature ? [CBSE D 02]

17. What is an intrinsic semiconductor ? Why does the conductivity of an intrinsic semiconductor increase with the rise of temperature ? [Haryana 93]

18. Define the terms 'potential barrier' and 'depletion region' for a *p*-*n* junction diode. Explain how the thickness of depletion region will change when the *p*-*n* junction diode is (*i*) forward biased (*ii*) reverse biased [CBSE D 06]

19. With the help of a suitable diagram, explain the formation of depletion region and potential barrier in a *p*-*n* junction. How does its width change when the junction is (*i*) forward biased, and (*ii*) reverse biased ? [CBSE OD 09 ; D 11, 14C, 15]

20. In the circuits shown in Fig. 14.212, which one of the two diodes is forward biased and which is reverse biased ? [CBSE D 05]

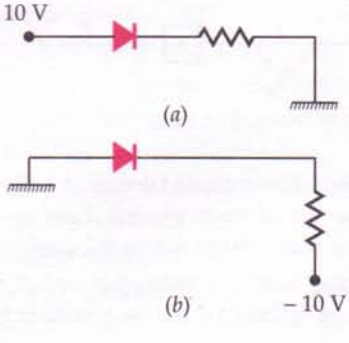


Fig. 14.212

21. Write briefly the important processes that occur during the formation of *p-n* junction. With the help of necessary diagrams, explain the term 'barrier potential' [CBSE F 15]

22. (*i*) With the help of circuit diagrams, distinguish between forward biasing and reverse biasing of *p-n* junction diode.

(*ii*) Draw *V–I* characteristics of a *p-n* junction diode in (*a*) forward bias, (*b*) reverse bias.

[Himachal 05 ; CBSE OD 05C, 09]

23. Draw the characteristic (*V-I*) curve of a junction diode. Write down in your graph the approximate values of voltage and current. On the basis of your graph, explain how a junction diode acts as a rectifier. [ISCE 90, 91]

24. What is a *p-n* junction diode ? Define the term dynamic resistance for the junction diode.

[Haryana 99]

25. Explain (*i*) forward biasing, (*ii*) reverse biasing of the *p-n* junction diode. With the help of a circuit diagram, explain the use of this device as a half-wave rectifier.

[ISC 2000 ; Himachal 04 ; CBSE OD 06]

26. Explain, with the help of a circuit diagram, the working of a *p-n* junction diode as a half-wave rectifier. [CBSE OD 14]

27. Draw a circuit diagram of full-wave rectifier. Explain its working principle. Draw the input / output, wave-forms indicating clearly the functions of the two diodes used.

[Punjab 02, 04 ; CBSE D 14C, 15C ; OD 08, 11]

28. An a.c. signal is fed into two circuits *X* and *Y* and the corresponding output in the two cases have the waveforms shown in Fig. 14.213. Name the circuits *X* and *Y*. Also draw their detailed circuit diagrams.

[CBSE Sample Paper 11]

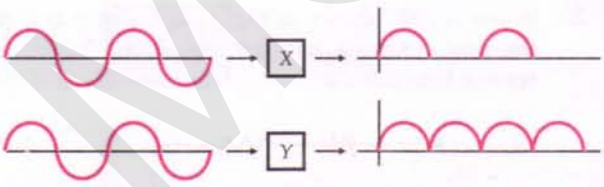


Fig. 14.213

29. How is a Zener diode fabricated ? What causes the setting up of high electric field even for small reverse bias voltage across the diode ?

Describe, with the help of a circuit diagram, the working of Zener diode as a voltage regulator.

[CBDE OD 15]

30. The output of an unregulated d.c. power supply is to be regulated. Name the device that can be used for this purpose and draw the relevant circuit diagram. [CBSE D 05C, 06C]

31. What is a Zener diode ? How is it represented symbolically ? With the help of a circuit diagram, explain the use of Zener diode as a voltage stabilizer. [Haryana 01 ; CBSE OD 01C]

32. Draw *V-I* characteristics of a zener diode. Explain with the help of a circuit diagram how a zener diode can be used as a voltage regulator.

[CBSE OD 08, 09]

33. Show the biasing of a photo-diode with the help of a circuit diagram. Draw graphs to show variations in reverse bias currents for different illumination intensities. [CBSE D 04, 05C]

34. Explain, with the help of a circuit diagram, the working of a photo-diode. Write briefly how it is used to detect the optical signals.

[CBSE D 13 ; OD 14C]

35. With the help of a diagram, show the biasing of a light emitting diode (LED). Give its two advantages over conventional incandescent lamps. [CBSE D 04]

36. What is a light emitting diode ? With the help of a circuit diagram, explain its action.

37. What is a solar cell ? Briefly explain the construction and working of a solar cell. Draw its *V-I* characteristic.

38. Describe briefly with the help of a circuit diagram, the paths of current carriers in an *n-p-n* transistor with emitter-base junction forward biased and base-collector junction reverse biased. [CBSE OD 12]

39. Describe briefly with the help of a circuit diagram, how the flow of current carriers in a *p-n-p* transistor is regulated with emitter-base junction forward biased and base-collector junction reverse biased.

[CBSE OD 12]

40. In Fig. 14.214, is (*i*) the emitter, and (*ii*) the collector forward or reverse biased ? With the help of a circuit diagram, explain the action of an *n-p-n* transistor. [CBSE D 01C]

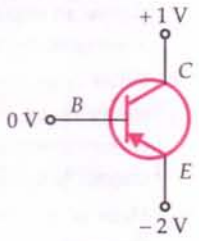


Fig. 14.214

41. Draw a circuit diagram of a transistor amplifier in CE configuration. Under what condition does the transistor act as an amplifier ?

Define the terms : (*i*) Input resistance and (*ii*) Current amplification factor. How are these determined using typical input and output characteristics ? [CBSE OD 14 ; D 15]

42. Draw typical output characteristics of an *n-p-n* transistor in *CE* configuration. Show how these characteristics can be used to determine output resistance. [CBSE OD 13]

43. Derive a relation between current gain of a common base amplifier and current gain of a common emitter amplifier. [Himachal 04]

44. When is a transistor said to be in active state ? Draw a circuit diagram of *p-n-p* transistor and explain how it works as a transistor amplifier. Write clearly, why in the case of a transistor (*i*) the base is thin and lightly doped and (*ii*) the emitter is heavily doped. [CBSE OD 15]

45. Draw a circuit diagram of a CE transistor amplifier. Briefly explain its working and write the expression for (*i*) current gain (*ii*) voltage gain of the amplifier. [CBSE OD 15]

46. Draw the labelled circuit diagram of a common-emitter transistor amplifier. Explain clearly how the input and output signals are in opposite phase. [Haryana 03 ; CBSE OD 05C, 08 ; OD 08]

47. Draw a labelled circuit diagram of a common base amplifier using an *n-p-n* transistor. Name the purpose for which common base transistor amplifier is preferred over common emitter transistor amplifier. [CBSE OD 03]

48. State briefly the underlying principle of a transistor oscillator. Draw a circuit diagram showing how the feedback is accomplished by inductive coupling. Explain the oscillator action. [CBSE OD 08]

49. Draw the transfer characteristics of a base biased transistor in its common emitter configuration. Explain briefly the meaning of the term 'active region' in these characteristics. For what practical use, do we use the transistor in this 'active region' ? [CBSE Sample Paper 08]

50. What do we understand by the cut off, active and saturation states of the transistor ? In which of these states does the transistor not remain when being used as a switch ? [CBSE Sample Paper 08]

51. Explain the advantages and disadvantages of semiconducting devices compared to vacuum tube devices. [Punjab 02, 03]

52. Give the logic symbol and a truth table for an OR gate. Explain, with the help of a circuit, how is this gate realised in practice. [CBSE D 97, 04 ; OD 2000 C]

53. Give the logic symbol and truth table for AND gate. Explain, with the help of a circuit diagram, how this gate realised in practice. [CBSE D 97, 04 ; OD 2000C]

54. Give the logic symbol and truth table for NOT gate. Explain, with the help of a circuit diagram, how is this gate realised in practice. [CBSE D 97]

55. Write the truth-table of a two input NAND gate. Explain, using a logic circuit, how a NAND gate can be converted into a NOT gate. [CBSE D 98C]

56. Draw the logic symbol of a 2-input NAND gate. Write down its truth table. [CBSE D 2000]

57. The output of a 2-input AND gate is fed to a NOT gate. Give the name of the combination and its logic symbol. Write down its truth table. [CBSE D 09]

58. Write the truth table of a 2-input NOR gate. Explain, using a logic circuit, how a NOR gate can be converted into an AND gate. [CBSE OD 98C]

59. A logic gate is obtained by applying output of OR gate to a NOT gate. Name the gate so formed. Write the symbol and truth table of this gate. [CBSE OD 04C ; F 09]

60. Draw the logic symbol of a 2-input NOR gate. Write down its truth table. [CBSE D 2000]

61. Draw and explain the output waveform across the load resistor *R*, if the input waveform is as shown in the given Fig. 14.215.

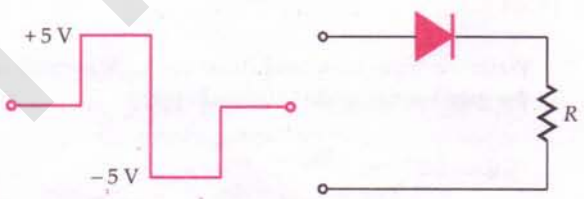


Fig. 14.215

62. If the output of a 2 input NOR gate is fed as both inputs *A* and *B* to another NOR gate, write down a truth table to find the final output, for all combinations of *A*, *B*. [CBSE D 08]

63. The given inputs *A*, *B* are fed to a 2-input NAND gate. Draw the output wave form of the gate. [CBSE D 08 ; OD 14C]

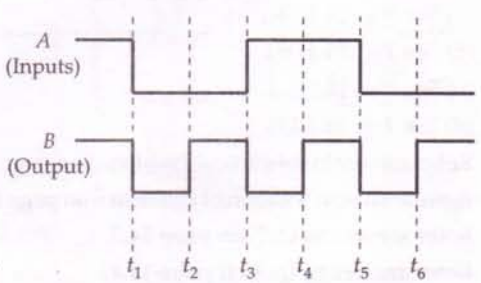


Fig. 14.216

64. The inputs A and B are inverted by using two NOT gates and their outputs are fed to the NOR gate as shown below.

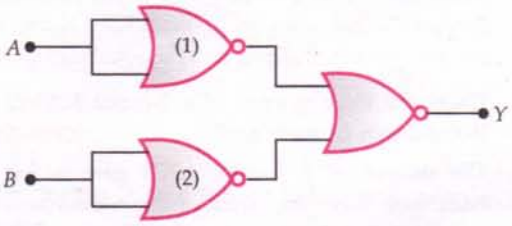


Fig. 14.217

Analyse the action of the gates (1) and (2) and identify the logic gate of the complete circuit so obtained. Give its symbol and the truth table.

[CBSE OD 08 ; D 15C]

65. Write the truth table and draw the logic symbol of the gate given below : [CBSE F 08]

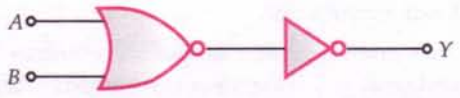


Fig. 14.218

66. Write the truth table and draw the logic symbol of the gate for the circuit shown below :

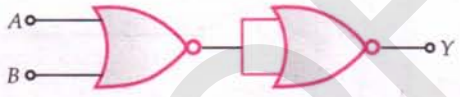


Fig. 14.219

67. Identify the gate equivalent to the 'dotted box' shown here and give its symbol and truth table.

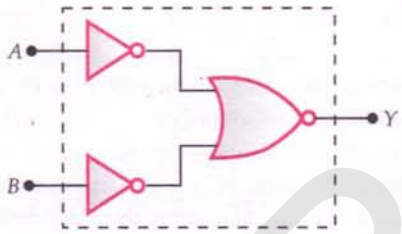


Fig. 14.220

The input 'A', shown here, is used with another unknown input 'B' in this set-up. If the output 'Y' has the form shown, give the intervals over which the input 'B' is in its '*high*' state. [CBSE D 08C]

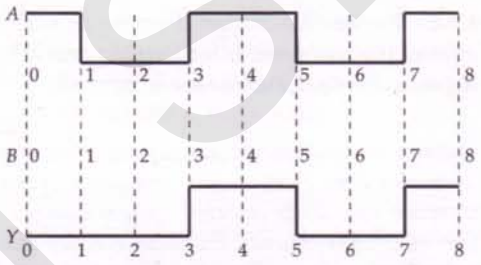


Fig. 14.221

68. (*a*) What is an 'integrated circuit (I.C.)' ? Distinguish between (*i*) linear I.C. and (*ii*) digital I.C.

(*b*) Identify the equivalent gate for the following circuit and write its truth table. [CBSE F 15]

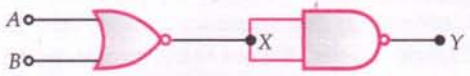


Fig. 14.222

Answers

1. Refer answer to Q. 3 on page 14.2.
2. Refer answer to Q. 12 on page 14.7.
3. (*a*) See Fig. 14.10(*a*).
   (*b*) See Fig. 14.11(*b*).
   (*c*) See Fig. 14.11(*c*).
   (*d*) See Fig. 14.10(*b*).
4. Refer answer to solution of Problem 5 on page 14.70.
5. Refer answer to solution of Problem 6 on page 14.70.
6. Refer answer to Q. 7 on page 14.3.
7. Refer answer to Q. 8 on page 14.4.
8. Refer answer to Q. 18 on page 14.11.
9. Refer answer to Q. 13 on page 14.8
10. If pentavalent impurity atoms of Bi, Sb or P are doped in a tetravalent crystal Ge or Si, we get n-type semiconductor. Electrons are the major charge carriers in it. For energy band diagram, see Fig. 14.11(*b*).
11. If trivalent impurity atoms of B, Al or In are doped in a pure semiconductor of Si or Ge, we get a p-type semiconductor. Holes are the major charge carriers in it. For energy band diagram see Fig. 14.11(*c*).
12. For energy band diagram, see Fig. 14.11(*c*).

    Expression for conductivity of a p-type semiconductor. A p-type semiconductor has holes as the majority charge carriers.

$\therefore \quad I = I_h = en_h A v_h$

Also $R = \rho \frac{l}{A} \quad \therefore \quad V = RI = \rho \frac{l}{A} . en_h A v_h$

$$E = \frac{V}{l} = \rho e n_h v_h = \rho e n_h . \mu_h E \quad \left[\because \mu_h = \frac{v_h}{E} \right]$$

$\therefore$ Conductivity, $\rho = \frac{1}{\rho} = en_h \mu_h$

13. Refer to the solutions of Problems 6 and 7 on page 14.70.
14. Refer answer to Q. 16 on page 14.9.
15. Refer answer to Q. 17 on page 14.11.
16. For energy band diagram, see Fig. 14.17(*b*). The forbidden energy gap does not change with temperature.
17. Refer answer to Q. 19 on page 14.12.
18. Refer to the solutions of Problem 13 on page 14.69 and Problem 15 on page 14.70.
19. Refer to the solutions of Problem 13 on page 14.69 and Problem 15 on page 14.70.
20. (*a*) The *p-n* junction is reverse biased.
    (*b*) The *p-n* junction is forward biased.
21. Refer to the solution of Problem 13 on page 14.69.
22. Refer to the solutions of Problems 16 and 17 on page 14.72.
23. See Fig. 14.21 and its explanation on page 14.18.
24. Refer to points 17 and 19 of Glimpses.
25. Refer answer to Q.25 on page 14.18 and Q.26 on page 14.19.
26. Refer answer to Q. 26 on page 14.19.
27. Refer answer to Q. 27 on page 14.19.
28. *X* is a half-wave rectifier, see Fig. 14.22 on page 14.19.
    Y is a full-wave rectifier, see Fig. 14.24 on page 14.19.
29. In a zener diode, both *p*- and *n*-sections are heavily doped with impurities. Due to this, the depletion layer becomes very thin ($< 10^{-6}$ m). Even a small reverse bias voltage sets up a very high electric field ($E = V / d$).
    For circuit diagram and working of zener diode, refer to the solution of Problem 26 on page 14.74.
30. Zener diode is used to regulate unregulated dc. See Fig. 14.32 on page 14.21.
31. Refer to the solution of Problem 26 on page 14.74.
32. Refer to the solution of Problem 26 on page 14.74.
33. See Fig. 14.35 and Fig. 14.36 on page 14.22.
34. Refer answer to Q. 32 on page 14.22.
35. Refer answer to Q. 33 on page 14.23.
36. Refer answer to Q. 33 on page 14.23.
37. Refer answer to Q. 34 on page 14.23.
38. Refer answer to Q. 37 on page 14.31.
39. Refer answer to Q. 38 on page 14.31.
40. Refer answer to Q. 37 on page 14.31.
    For the given *p-n-p* transistor,
    (*a*) the emitter is reverse biased
    (*b*) the collector is forward biased.
41. See Fig. 14.74 on page 14.38.
    Condition. For a transistor to act as an amplifier, it must be operated close to the centre of its active region.
    Input resistance, $R_i = \left[\frac{\Delta V_{BE}}{\Delta I_B} \right]_{V_{CE} = \text{constant}}$
    Its value is determine from the slope of I_B versus V_{BE} curve at constant V_{CE}.
    Current amplification factor,
    $$\beta_{ac} = \left[\frac{\Delta I_C}{\Delta I_B} \right]_{V_{CE} = \text{constant}}$$
    Its value is determined from the I_C *vs.* V_{CE} curves plotted different values of I_B.
42. Refer answer to Q. 41 on page 14.33.
43. Refer answer to Q. 40 on page 14.32.
44. Refer answer to Q. 48 on page 14.39.
    Base is thin so that there are few majority charge carriers in it.
    Emitter is heavily doped so that it supplies a large number of majority charge carriers.
45. Refer to the solution of Problem 39(*d*) on page 14.77. For expressions, refer answer to Q. 41 above.
46. Refer answer to Q. 47 on page 14.38.
47. See Fig. 14.72, *CB* configuration is preferred when low voltage is required or when we use single stage amplifier.
48. Refer answer to Q. 49 on page 14.48.
49. Refer answer to Q. 42 on page 14.35. For using transistor as an amplifier, we use the active region of the transfer characteristic.
50. Refer answer to Q. 42 on page 14.35. The transistor does not remain in active state when being used as a switch.
51. Refer answer to Q. 35 on page 14.25.
52. Refer answer to Q. 54 on page 14.52.
53. Refer answer to Q. 55 on page 14.53.
54. Refer answer to Q. 56 on page 14.54.
55. Refer answer to Q. 57 on page 14.55.
56. Refer answer to Q. 57 on page 14.55.
57. Refer answer to Q. 57 on page 14.55.

58. Refer answer to Q. 58 on page 14.56.
59. Refer answer to Q. 58 on page 14.56.
60. Refer answer to Q. 58 on page 14.56.
61. When the input voltage is + 5 V, the diode gets forward biased, the output across R is + 5 V, as shown in Fig. 14.223. When the input voltage is – 5 V, the diode gets reverse biased. No output is obtained across R.

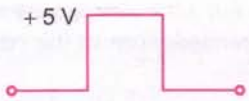


Fig. 14.223

62. Refer to the solution of Example 48 on page 14.59.
63. See Fig. 14.106 on page 14.56.
64. Refer to the solution of Example 49 on page 14.59.
65. Refer to the solution of Example 53 on page 14.61.
66. Refer to the solution of Example 48 on page 14.59.
67. The dotted box acts as an AND gate (For explanation, refer to the solution of Example 50 on page 14.60. The input B must atleast be high in the time intervals $3 < t < 5$ and $7 < t < 8$.
68. (*a*) A miniature electronic circuit, consisting of many passive components like R and C and active devices like diode and transistor, fabricated within a single semiconductor chip is called an integrated circuit.

(*i*) Linear ICs are used for analog functions.

(*ii*) Digital or non-linear ICs are used for digital or switching functions.

(*b*) X = output of NOR gate

Y = output of NOT gate made from NAND gate.

Truth table

A	B	X	Y
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Clearly, $A + B = Y$. So the given circuit is equivalent to an OR gate.

TYPE C : LONG ANSWER QUESTIONS (5 marks each)

1. What are intrinsic semiconductors ? On the basis of valence bond model, explain the mechanism of conduction in intrinsic semiconductors. How do holes act as positive charge carriers ?
2. Explain the formation of energy bands in solids. On the basis of energy band diagrams, distinguish between (*i*) a metal, (*ii*) an insulator and (*iii*) a semiconductor. [Punjab 2000, 04 ; CBSE D 96 ; OD 06]
3. Explain how an intrinsic semiconductor can be converted into (*i*) n-type and (*ii*) p-type semiconductor.

   Give one example of each and their energy band diagrams. [CBSE OD 94 ; D 01C]
4. (*a*) Explain the formation of depletion layer and potential barrier in a p-n junction.

   (*b*) In Fig. 14.224, the input waveform is converted into the output waveform by a device 'X'. Name the device and draw its circuit diagram.

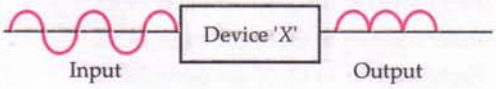


Fig. 14.224

   (*c*) Distinguish between a conductor, a semiconductor and an insulator on the basis of energy band diagrams. [CBSE D 10]
5. (*a*) Draw the circuit diagrams of a p-n junction diode in (*i*) forward bias, (*ii*) reverse bias. How are these circuits used to study the V-I characteristics of a silicon diode ? Draw the typical V-I characteristics. How do we infer, from these characteristics, that a diode can be used to rectify ac ? [CBSE D 14]

   (*b*) What is a light emitting diode (LED) ? Mention two important advantages of LEDs over conventional lamps. [CBSE OD 10]
6. (*a*) Describe briefly, with the help of a diagram, the role of the two important processes involved in the formation of a p-n junction.

   (*b*) Name the device which is used as a voltage regulator. Draw the necessary circuit diagram and explain its working. [CBSE OD 12 ; D 14C]
7. Explain how the heavy doping of the p and n sides of a p-n junction diode helps in internal field emission (or zener breakdown) even with a reverse bias voltage of few volts only.

   Draw the general shape of the V-I characteristics of a zener diode. Discuss how the nature of these characteristics led to the use of a zener diode as a voltage regulator. [CBSE OD 07C ; F 13]

8. (*i*) How is a zener diode fabricated so as to make it a special purpose diode ? Draw *I-V* characteristics of zener diode and explain the significance of breakdown voltage.

(*ii*) Explain briefly, with the help of a circuit diagram, how a *p-n* junction diode works as a half wave rectifier. [CBSE D 09]

9. (*a*) Differentiate between three segments of a transistor on the basis of their size and level of doping.

(*b*) How is a transistor biased to be in active state ?

(*c*) With the help of necessary circuit diagram, describe briefly how *n-p-n* transistor in CE configuration amplifies a small sinusoidal input voltage. Write the expression for the ac current gain. [CBSE D 14]

10. (*a*) Draw the circuit diagram of an *n-p-n* transistor with emitter-base junction forward biased and collector-base junction reverse biased. Describe briefly how the motion of charge carriers in the transistor constitutes the emitter current (I_E), the base current (I_B) and the collector current (I_C). Hence deduce the relation $I_E = I_B + I_C$.

(*b*) Explain with the help of circuit diagram how a transistor works as an amplifier. [CBSE OD 14C]

11. (*a*) Draw the circuit arrangement needed for studying the input and output characteristics of an *n-p-n* transistor in common emitter configuration. Draw the typical shape of these input and output characteristics. Why is it usually enough to determine only one input characteristics ?

(*b*) The small signal current gain (β_{ac}) of a transistor, can be taken as nearly equal to its dc current amplification factor (β_{dc}). Why ?

[CBSE OD 01, 06, 08C ; D09]

12. Draw the circuit diagram for the *n-p-n* transistor in common emitter configuration. With the help of typical input, output characteristics, write the expressions for (*i*) input resistance (*ii*) output resistance and (*iii*) current amplification factor.

When would you prefer to use a transistor as a common base amplifier ?

[CBSE D 07C, 10 ; OD 10 ; F 13]

13. Draw a circuit diagram of an *n-p-n* transistor with its emitter base junction forward biased and base collector junction reverse biased. Describe briefly its working.

Explain how a transistor in active state exhibits a low resistance at its emitter base junction and high resistance at its base collector junction.

[CBSE F 09]

14. (*a*) Fig. 14.225 shows the input waveform which is converted by a device '*X*' into an output waveform. Name the device and explain its working using the proper circuit. Derive the expression for its voltage gain and power gain.

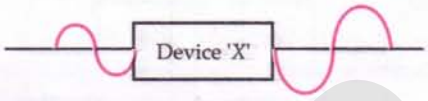


Fig. 14.225

(*b*) Draw the transfer characteristic of a base biased transistor in CE configuration. Explain clearly which region of the curve is used in an amplifier. [CBSE D 15C]

15. With the help of a labelled circuit diagram, explain how an *n-p-n* transistor can be used as an amplifier in common-emitter configuration. Write an expression for its voltage gain. Explain how the input and output voltages are out of phase by 180° for a common-emitter transistor amplifier.

[CBSE D 09, 10 ; OD 10 ; F 06]

16. Draw a simple circuit of a CE transistor amplifier. Explain its working. Show that the voltage gain, A_V, of the amplifier is given by

$$A_V = -\frac{\beta_{ac} R_L}{r_i},$$

where β_{ac} is the current gain, R_L is the load resistance and r_i is the input resistance of the transistor. What is the significance of the negative sign in the expression for the voltage gain ? [CBSE D 12]

17. The set up, shown in Fig. 14.226, can produce an a.c. output without any external input signal, identify the components *X* and *Y* of this set up. Draw the circuit diagram for this set up and briefly describe its working. [CBSE Sample paper 11]

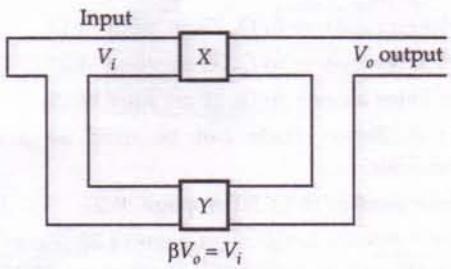


Fig. 14.226

18. (*a*) Draw the circuit diagram of a full wave rectifier using *p-n* junction diode. Explain its working and show the output, input waveforms.

(*b*) Show the output waveforms (*Y*) for the inputs *A* and *B* shown in Fig. 14.227 of (*i*) OR gate (*ii*) NAND gate. [CBSE D 12]

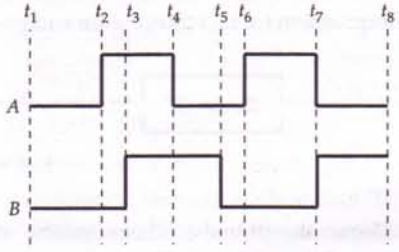


Fig. 14.227

19. (*a*) Describe briefly with the help of a circuit diagram how an *n-p-n* transistor is used to produce self-sustained oscillations.

(*b*) Identify the logic gate represented by the circuit as shown and write its truth table [CBSE OD 10]

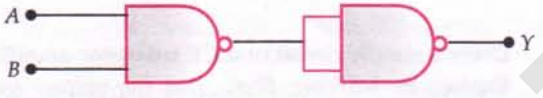


Fig. 14.228

20. (*a*) Explain briefly the principle on which a transistor-amplifier works as an oscillator. Draw the necessary circuit diagram and explain its working.

(*b*) Identify the equivalent gate for the following circuit and write its truth table. [CBSE OD 12]

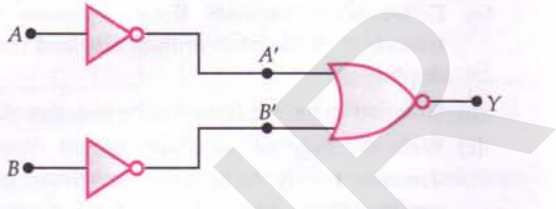


Fig. 14.229

21. (*a*) Why is the base region of a transistor kept thin and lightly doped ?

(*b*) Draw the circuit diagram of the 'set-up' used to study the characteristics of a *n-p-n* transistor in its common emitter configuration. Sketch the typical (*i*) Input characteristics and (*ii*) Output characteristics for this transistor configuration.

(*c*) How can the output characteristics be used to calculate the 'current gain' of the transistor ? [CBSE D 13C]

Answers

1. Refer answer to Q. 5. on page 14.3.
2. Refer answer to Q. 11, 12 on page 14.6 and 14.7.
3. Refer answer to Q. 9 on page 14.4.
4. (*a*) Refer answer to Q. 21 on page 14.15.

   (*b*) The device *X* is a full wave rectifier. See Fig. 14.24 on page 14.19.

   (*c*) Refer to the solution of Problem 5 on page 14.70.
5. (*a*) Refer answer to Q. 23 on page 14.17.

   (*b*) Refer answer to Q. 33 on page 14.23.
6. (*a*) Refer answer to Q. 21 on page 14.15.

   (*b*) A Zener diode can be used as a voltage regulator.

   Refer answer to Q. 30 on page 14.21.
7. Refer answer to Q. 29 on page 14.20 (Zener breakdown) and answer to Q. 30 on page 14.21 (zener diode as a voltage regulator).
8. (*i*) Refer answer to Q. 30 on page 14.21.

   (*ii*) Refer answer to Q. 26 on page 14.19.
9. Refer to the solution of Problem 39 on page 14.77.
10. (*a*) Refer answer to Q. 37 on page 14.31.

    (*b*) Refer to the solution of Problem 39(*d*) on page 14.77.
11. Refer answer to Q. 41 on page 14.33.
12. Refer answer to Q. 41 on page 14.33 and refer to the solution of Problem 39 on page 14.67.
13. Refer answer to Q. 37, 43 on pages 14.31 and 14.36.
14. (*a*) The device is common emitter amplifier. For its working and circuit diagram, refer to the solution of Problem 39(*d*) on page 14.77.

    Input sinusoidal voltage,

$$V_i = \Delta I_B (R_B + r) = \Delta I_B r$$

$$\text{Current gain, } \beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \Rightarrow \Delta I_C = \beta_{ac} \Delta I_B$$

$$\Delta V_{CE} = -R_L \Delta I_C = -R_L \beta_{ac} \Delta I_B = V_0$$

$$\therefore \text{ Voltage gain, } A_v = \frac{V_o}{V_i} = -\beta_{ac} \frac{R_L}{r}$$

$$\text{Power gain, } A_p = \beta_{ac} A_v = \beta_{ac}^2 \frac{R_L}{r}.$$

(*b*) Refer to the solution of Problem 39(*c*) on page 14.77.

15. Refer answer to Q. 47 on page 14.38.

16. Refer answer to Q. 47 on page 14.38. The negative sign in the expression for the voltage gain shows that output voltage and input voltage have a phase difference of π rad.

17. The given set up represents the principle of a transistor working as an oscillator.

Here X = Transistor amplifier ; Y = Feedback circuit

For its circuit diagram and working, refer answer to Q. 49 on page 14.48.

18. (*a*) Refer answer to Q. 27 on page 14.19.

(*b*)

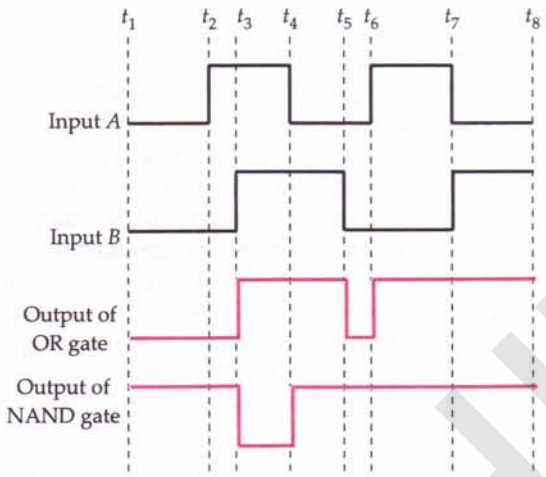


Fig. 14.230

19. (*a*) Refer answer Q. 49 on page 14.48.

(*b*) Refer to the solution of Example 52(*i*) on page 14.60.

20. (*a*) Refer answer to Q. 49 on page 14.48.

(*b*) Refer to the solution of Example 50(*ii*) on page 14.60.

21. (*a*) The base region of a transistor is thin and lightly doped so that most of the majority charge carriers coming from the emitter into the base immediately get collected by the collector, without undergoing electron-hole recombination in the base region. This ensures that base current I_B is very small as compared to emitter current I_E.

(*b*) For circuit diagram and input and output characteristics of an *n-p-n* transistor in *CE* configure, see Figs. 14.66, 14.67 and 14.68.

(*c*) The current gain (β) of a transistor in common emitter configuration is

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

ΔI_C and ΔI_B can be obtained from any two curves in the output characteristics.

TYPE D : VALUE BASED QUESTIONS (4 marks each)

1. A semiconductor device is used as a rectifier that allows the voltage to flow in positive direction and a very small value in the reverse direction. Now a days, there is a problem of supply of less voltage that damages the household appliances. You are asked to give the technique to save the appliances in use.

(*a*) What can you think to solve the situation ?

(*b*) Can a diode be fabricated in terms of doping and choice of material to control the input voltage to save your appliances from damage ?

2. (*a*) A child uses a semiconductor device in listening radio and seeing pictures on TV. He was asked to suggest the techniques as the cost of LPG/CNG is going up, to cope with future situations.

(*b*) What are the values developed by the child ?

(*c*) What may be the suitable semiconductor material used for utilization of maximum solar energy ?

3. Puneet was enjoying TV programme at his home with his family at night. Suddenly the light went off causing darkness all over. Mother asked Puneet to bring candle along with matchstick from the kitchen to put the TV switch off. Puneet at once picked the mobile phone and pressed the button lighting up the surrounding. Her mother was surprised and asked where the light was coming from. Puneet proudly showed her that mobile.

(*a*) Which values were displayed by Puneet.

(*b*) Which material is used in LED ?

4. Sabby and Sonali wanted to purchase a new TV set. They visited electronic shops to look for some branded TVs. The dealer showed them both LCD and LED TVs. Now they were confused which set to buy. Finally after discussing with friends, reading relevant literature and searching the internet, they decided to purchase an LED.
   (*a*) Which value is being highlighted by Sabby and Sonali ?
   (*b*) What is difference between LED and LCD ?

5. Lakshay was reading semiconductors in Physics. His teacher explained that electronic components operate at very low voltage. But at home he daily saw his father using wall socket for charging mobile (220 V). Confused Lakshay put his doubt in front of his teacher and was satisfied. Next day, he went to school and shared the information with his classmates.
   (*a*) Name the values displayed by Lakshay.
   (*b*) What is the principle of a charger ?

Answers

1. (*a*) Critical thinking.
   (*b*) Yes, it is Zener diode which is specially designed to operate in the reverse breakdown region continuously and can be used as a voltage regulator.

2. (*a*) Awareness of social problems and generating new idea with fluency.
   (*b*) The suitable semiconductors for the fabrication of solar cells are Si, GaAs, CdTe, etc., because of their suitable bandgap (1.0 to 1.45 eV) and high optical absorption.

3. (*a*) Critical thinking and resourcefulness.
   (*b*) $GaAs_{0.6}P_{0.4}$ is used for red LED while GaAs is used for infrared LED.

4. (*a*) Interpretation skill.
   (*b*) LED is a forward biased junction diode which spontaneously converts the biasing electrical energy into optical energy like visible light. Liquid crystals are liquids which show some degree of molecular order. Liquid crystal displays (LCDs) make use of light-polarizing properties of such crystals. When no voltage is applied to the crystal, it twists the light polarization through 90° and polarized light is reflected by a mirror. When voltage is applied, there is no twisting, the light does not pass through second polarizer and is not reflected.

5. (*a*) Scientific thinking.
   (*b*) A battery charger is based on the rectifying action of junction diodes.

COMPETITION SECTION

Semiconductor Devices and Digital Circuits

GLIMPSES

1. **Electronic devices.** Any device whose action is based on the controlled flow of electrons through it is called an ***electronic device***. The branch of physics that deals with the study of these electronic devices is called ***electronics***. The electronic devices are of *two* types :

   (*i*) Vacuum tubes

   (*ii*) Solid-state electronic devices.

2. **Vacuum tubes.** These include vacuum diode, triode, tetrode, etc. In a vacuum tube, electrons obtained from a heated cathode are controlled by varying voltages between its different electrodes. These devices are bulky, consume high power , operate generally at high voltages, have limited life and low reliability.

3. **Solid-state electronic devices.** In such devices, the charge carriers flow through solid-state semiconductors. These devices include junction diodes, transistors and integrated circuits. These are small in size, consume low power, operate at low voltages, have long life and high reliability.

4. **Classification of solids on the basis of their resistivities.** Metals have low resistivity (10^{-2} to $10^{-8}\ \Omega$m), insulators have high resistivity ($>10^{8}\ \Omega$m), while semiconductors have intermediate values (10^{5} to $10^{0}\ \Omega$m) of resistivity.

5. **Semiconductors.** They have much higher resistivity than metals. Their temperature coefficient of resistivity (α) is both negative and high. They have considerably lower number density of charge carriers than metals. Semi-conductors may be elemental (Si, Ge) and compound (GaAs, CdS, etc.)

6. **Energy bands in solids.** In an isolated atom, the electrons occupy well defined discrete energy levels. But due to interatomic interactions in a crystal, the electrons of the outer shells are forced to have energies different from those in isolated atoms. Each energy level splits into a number of energy levels forming a continuous band.

   An enormously large number of energy levels closely spaced in a very small energy range constitute an ***energy band***. The allowed energy bands are separated by regions in which energy levels cannot exist. These forbidden regions are called *band gaps* or *energy gaps*. The highest energy band occupied by the valence electrons is called the *valence band* and the next empty allowed band is called the *conduction band*.

7. **Fermi level.** The highest energy level filled with electrons at absolute zero is called Fermi level and the energy corresponding to the Fermi level is called Fermi energy.

8. **Distinction between metals, insulators and semiconductors on the basis of band theory.**

   (*i*) ***Metals.*** In metals, either the conduction band is partially filled or the valence and conduction bands partly overlap.

   Here $E_g = 0$.

   This makes available a large number of free electrons for electric conduction. So metals have high conductivity or low resistivity.

   (*ii*) ***Insulators.*** Here the conduction band is empty and the valence band is filled. The forbidden energy gap is large ($E_g > 3$ eV). Electrons cannot be excited from the valence band to the conduction band even by applying a strong electric field. Therefore, no electrical conduction is possible.

(iii) ***Semiconductors.*** The empty conduction band is separated from the filled valence band by a small energy gap (E_g <3 eV). Some electrons of the valence band easily get thermally excited to the conduction band and can conduct electricity. So semiconductors acquire small conductivity even at room temperature.

9. Intrinsic semiconductors. The pure semiconductors in which the electrical conductivity is totally governed by the electrons excited from the valence band to the conduction band and in which no impurity atoms are added to increase their conductivity are called intrinsic semiconductors and their conductivity is called intrinsic conductivity. Electrical conduction in pure semiconductors occurs by means of electron-hole pairs. In an intrinsic semiconductor,

$$n_e = n_h = n_i$$

where,

n_e = the free electron density in conduction band,

n_h = the hole density in valence band, and

n_i = the intrinsic carrier concentration.

10. Doping. The process of deliberate addition of a desirable impurity to a pure semiconductor so as to increase its conductivity is called doping. The impurity atoms added are called dopants.

Dopants are of *two* types :

(i) ***Pentavalent dopants*** such as As, Sb and P. These are also called ***donors***.

(ii) ***Trivalent dopants*** such as In, B and Al. These are also called ***acceptors***.

11. Extrinsic semiconductors. A semiconductor doped with suitable impurity atoms so as to increase its conductivity is called an extrinsic semiconductor. Extrinsic semiconductors are of two types :

(i) *n-type semiconductors*, and

(ii) *p-type semiconductors*.

12. *n*-type semiconductors. The pentavalent impurity atoms are called donors because they donate electrons to the host crystal and the semiconductor doped with donors is called *n*-type semiconductor. In *n*-type semiconductors, electrons are the majority charge carriers and holes are the minority charge carriers. Thus

$$n_e \simeq N_D > n_h$$

13. *p*-type semiconductors. The trivalent impurity atoms are called acceptors because they create holes which can accept electrons from the nearby bonds. A semiconductor doped with acceptor type impurities is called a *p*-type semiconductor. In *p*-type semiconductor, holes are the majority carriers and electrons are the minority charge carriers. Thus

$$n_h \approx N_A > n_e$$

In any semiconductor,

$$n_e n_h = n_i^2$$

Moreover, the material on the whole is electrically neutral.

14. Holes. The vacancy or absence of electron in the bond of a covalently bonded crystal is called a hole. A hole serves a positive charge carrier.

15. Mobility. The drift velocity acquired by a charge carrier in a unit electric field is called its electrical mobility and is denoted by μ.

$$\mu = \frac{v}{E}$$

SI unit of $\mu = m^2 V^{-1} s^{-1}$

The mobility of an electron in the conduction band is greater than that of the hole (or electron) in the valence band.

16. Electrical conductivity of a semiconductor. If a potential difference V is applied across a conductor of length l and area of cross-section A, then the total current I through it is given by

$$I = eA(n_e v_e + n_h v_h)$$

where n_e and n_h are the electron and hole densities, and v_e and v_h are their drift velocities, respectively. If μ_e and μ_h are the electron and hole mobilities, then the conductivity of the semiconductor will be

$$\sigma = e(n_e \mu_e + n_h \mu_h)$$

and the resistivity will be

$$\rho = \frac{1}{e(n_e \mu_e + n_h \mu_h)}$$

The conductivity of an intrinsic semiconductor increases exponentially with temperature as

$$\sigma = \sigma_0 \exp\left(-\frac{E_g}{2k_B T}\right).$$

17. *p-n junction.* It is a single crystal of Ge or Si doped in such a manner that one half portion of it acts as *p*-type semiconductor and other half functions as *n*-type semiconductor. As soon as a

p-n junction is formed, the holes from the p-region diffuse into the n-region and electrons from n-region diffuse into p-region. This results in the development of ***potential barrier*** V_B across the junction which opposes the further diffusion of electrons and holes through the junction. The small region in the vicinity of the junction which is depleted of free charge carriers and has only immobile ions is called the ***depletion region***.

Symbol for a p-n junction diode.

18. Forward and reverse biasing of a p-n junction. If the positive terminal of a battery is connected to the p-side and the negative terminal to the n-side, then the p-n junction is said to be ***forward biased***. Both electrons and holes move towards the junction. A current, called forward current, flows across the junction. Thus a p-n junction offers a low resistance when it is forward biased.

If the positive terminal of a battery is connected to the n-side and negative terminal to the p-side, then p-n junction is said to be ***reverse biased***. The majority charge carriers move away from the junction. The potential barrier offers high resistance during the reverse bias. However, due to the minority charge carriers a small current, called reverse or leakage current, flows in the opposite direction. Thus a junction diode has almost a unidirectional flow of current.

The forward bias current is large (mA) while the reverse bias current is small (μA) in a p-n junction diode.

19. Dynamic resistance. The dynamic or ac resistance of a diode is the ratio of small change in applied voltage ΔV to the corresponding change in current ΔI. It is given by

$$r_d = \frac{\Delta V}{\Delta I}$$

20. Characteristic of a p-n junction diode. A graph showing the variation of current flowing through a p-n junction with the voltage applied across it (both when it is forward and reverse biased) is called the ***voltage-current*** or ***V-I characteristic*** of a p-n junction.

21. Rectification. The process of converting a.c. into d.c. is called rectification and the device used for this purpose is called a rectifier.

22. Junction diode as a rectifier. A junction diode conducts when forward biased and does not conduct when reverse biased. This unidirectional characteristic of the diode enables it to be used as a rectifier. A half-wave rectifier uses only a single diode while a full wave rectifier uses two diodes.

23. Zener diode. A junction diode specially designed to work only in the reverse breakdown region continuously is called a zener diode. The voltage drop across it is practically independent of current through it. So it can be used as a ***voltage regulator***.

24. Photodiode. It is a junction diode made from a photosensitive semiconducting material in such a way that light can fall on its junction. It is operated in a reverse bias condition. The photon excitation results in a change of reverse saturation current which helps us to measure light intensity.

25. Light emitting diode (LED). It is a forward biased p-n junction which spontaneously converts the biasing electrical energy into optical energy, like infra-red and visible light. It is made from a transulent semiconductor like GaAs or InP. LEDs are used in hand calculators, cash registers, digital clocks, etc.

26. Solar cell. It is a junction diode used to convert solar energy into electrical energy. It is based on photovoltaic effect (generation of voltage due to bombardment of light photons). The materials used for solar cells are Si and GaAs.

27. Junction transistor. It is a three terminal solid state device obtained by growing either a narrow section of p-type crystal between two relatively thicker sections of n-type crystals or a narrow section of n-type crystal between two thicker sections of p-type crystals. The first type is called n-p-n transistor and the second type is called p-n-p transistor. Each type of transistor has three components :

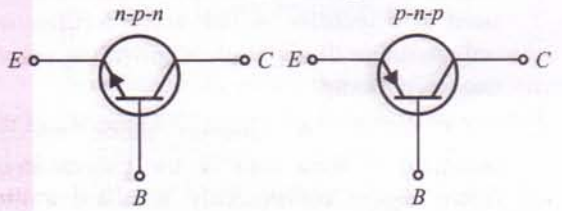
Emitter (E), Collector (C) and Base (B).

The base is very thin and lightly doped. The emitter is always forward biased and the collector is always reverse biased.

The emitter supplies a large number of majority charge carriers for the flow of current through the transistor.

The base controls the flow of majority charge carriers from emitter to cathode.

The collector collects the majority charge carriers for the transistor operation.



Circuit symbol of (*a*) *n-p-n* (*b*) *p-n-p* transistors.

28. Action of transistor. When the emitted-base junction is forward biased, majority charge carriers are pushed from emitter to base. Few electrons and holes recombine in the base region. Most of the majority charge carriers cross over to the reversed biased collector. Collector current I_c is always slightly less than the emitter current.

$$I_E = I_C + I_B, \quad \text{where } I_B \text{ is base current.}$$

29. Three configurations of a transistor. A transistor can be used in one of the following three configurations :

(*i*) Common-base (*CB*) circuit

(*ii*) Common-emitter (*CE*) circuit

(*iii*) Common-collector (*CC*) circuit.

30. Common-emitter characteristics of a transistor. These are the graphs between appropriate voltages and currents for a transistor when its emitter is taken as the common terminal and grounded (zero potential), base is the input terminal and collector is the output terminal. *Three* types of characteristic curves are studied :

(*i*) ***Input characteristic.*** It is the graph showing the variation of base current I_B with base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}.

The *input resistance* r_i of a transistor in *CE* configuration is defined as the ratio of the small change in the base-emitter voltage to the corresponding small change in base current, when the collector-emitter voltage is kept fixed.

$$r_i = \left[\frac{\Delta V_{BE}}{\Delta I_B}\right]_{V_{CE} = \text{constant}}$$

(*ii*) ***Output characteristic.*** It is the graph that shows the variation of collector current I_C with the collector-emitter voltage V_{CE} at constant base-current I_B.

The *output resistance* r_0 of a transistor in *CE* configuration is defined as the ratio of the small change in the collector-emitter voltage to the corresponding change in the collector-current when the base current is kept constant.

$$r_0 = \left[\frac{\Delta V_{CE}}{\Delta I_C}\right]_{I_B = \text{constant}}$$

(*iii*) ***Transfer characteristic.*** It is a graph showing the variation of collector current I_C with base current I_B at constant collector-emitter voltage V_{CE}.

31. Current gains of a transistor. Usually two current gains are defined :

(*i*) ***Common base current amplification factor or ac current gain*** α. It is the ratio of the small change in the collector current to the small change in the emitter current when the collector-base voltage is kept constant.

$$\alpha = \left[\frac{\Delta I_C}{\Delta I_E}\right]_{V_{CB} = \text{constant}}$$

(*ii*) ***Common emitter current amplification factor or ac current gain*** β. It is the ratio of the small change in the collector current to the small change in the base current when the collector-emitter voltage is kept constant.

$$\beta = \left[\frac{\Delta I_C}{\Delta I_B}\right]_{V_{CE} = \text{constant}}$$

32. Relations between α and β. The current gains α and β are related as

$$\alpha = \frac{\beta}{1+\beta} \quad \text{and} \quad \beta = \frac{\alpha}{1-\alpha}$$

33. Three states of a transistor. A transistor in a circuit can be in one of the three conditions :

(*i*) If the emitter-base junction is not forward-biased or if the bias is insufficient to start forward current across the junction while collector-base junction is reverse-biased, then the transistor is said to be in ***cutoff state.***

(*ii*) If the emitter-base junction is forward-biased and the collector base junction is reverse biased, a collector current flows in linear proportion with the base current. The transistor is said to be in the ***active state.***

(*iii*) If the emitter-base junction is heavily forward biased and the collector current produces such large drop across the load resistor that the base-collector junction also gets forward biased, then the transistor is said to be in ***saturation state***.

34. Transistor as a switch. A transistor can be used as a switch if it is biased in its cut off and saturation states only. The active state is forbidden when it is used as a switch.

35. Transistor as an amplifier. An amplifier is a circuit which is used for increasing the voltage, current or power of alternating form. A transistor operates as an amplifier when its emitter-base junction is forward biased while collector-base junction is reverse-biased. Transistor biased in this way is said to be in active state.

36. Common base transistor amplifier. (*i*) ***d.c. current gain.*** It is defined as the ratio of collector current to the emitter current.

$$\alpha_{dc} = \frac{I_C}{I_E}$$

(*ii*) ***a.c. current gain.*** It is defined as the ratio of the small change in collector current to the small change in emiiter current.

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$$

(*iii*) ***Voltage gain.*** It is defined as the ratio of the small change in output voltage to the small change in input voltage.

$$A_v = \frac{\Delta V_{CB}}{\Delta V_{EB}} = \frac{\Delta I_C \times R_o}{\Delta I_E \times R_i}$$

or $$A_v = \alpha_{ac} \cdot \frac{R_o}{R_i} = A_i \times A_r$$

(*iv*) ***Power gain.*** It is defined as the ratio of output power to input power.

$$A_p = \frac{\Delta V_{CB}}{\Delta V_{EB}} \times \frac{\Delta I_C}{\Delta I_E} = A_v \cdot A_i = A_v\, \alpha_{ac} = \alpha_{ac}^2 \cdot \frac{R_0}{R_i}$$

37. Common emitter transistor amplifier.

(*i*) ***d.c. current gain.*** It is defined as

$$\beta_{dc} = \frac{I_C}{I_B}$$

(*ii*) ***a.c. current gain.*** It is defined as

$$\beta_{ac} \text{ or } A_i = \frac{\Delta I_C}{\Delta I_B}$$

(*iii*) ***Voltage gain.*** It is defined as

$$A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}} = \beta_{ac} \cdot \frac{R_0}{R_i} = A_i \cdot A_r$$

(*iv*) ***Power gain.*** It is defined as

$$A_p = \frac{\text{Output power}}{\text{Input power}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{BE}} \cdot \frac{\Delta I_C}{\Delta I_B} = A_v \cdot \beta_{ac} = \beta_{ac}^2 \cdot \frac{R_o}{R_i}$$

(*v*) ***Transconductance*** (g_m). It is defined as the ratio of small change in collector current (ΔI_C) to the small change in input base-emitter voltage.

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}}$$

Its unit is Ω^{-1} or siemen (S). It depends on the geometry, doping levels and biasing of the transistor.

38. Oscillator. An oscillator is an electronic device which produces electric oscillations of constant frequency and amplitude. An *LC*-circuit is the basic oscillatory circuit. But its oscillations are damped. When a transistor is used an amplifier with positive feedback, it acts as an oscillator. Here the oscillations are set up in the tank or *LC*-circuit and feed-back energy is supplied in the correct phase by an inductance *L'* which is inductively coupled with the inductance *L* of the tank circuit.

The frequency of the oscillations in the tank circuit is

$$f = \frac{1}{2\pi\sqrt{LC}}$$

39. Analog circuits. These circuits process a signal (current or voltage) in the form of continuous, time-varying voltage or current. Such signals are called continuous or analog signals.

40. Digital circuits. These circuits, instead of using continuous signals, make use of discrete two-level or binary signals. Such signals are called digital signals. Here only two values (0 and 1) of the input and output voltage are permissible.

41. Logic gate. A logic gate is a digital circuit that has one or more inputs but only one output. It follows a logical relationship between input and output voltages.

42. Truth table. This table shows all possible input combinations and the corresponding outputs for a logic gate.

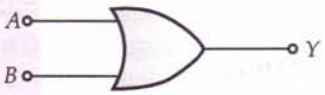
43. Boolean expression. It is a shorthand method to describe the function of a logic gate in the form of an equation or an expression. It also relates the all possible combinations of the inputs of a logic gate to the corresponding outputs.

44. Positive and negative logic. If in a system, the higher voltage level represents 1 and the lower voltage level represents 0, the system is called a positive logic. If the higher voltage level represents 0 and the lower voltage level represents 1, then the system is called a negative logic.

45. OR gate. It is a digital circuit having two or more inputs but only one output. It gives a high output if either input A or B or both are high (1) otherwise it gives low output (0). It is described by Boolean expression :

$$A + B = Y$$

Logic symbol of OR gate



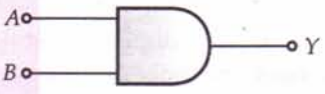
Truth table of OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

46. AND gate. It is a digital circuit having two or more inputs but only one output. It gives a high output (1) if inputs A and B are both high (1) otherwise it gives low output (0). It is described by the Boolean expression :

$$A . B = Y$$

Logic symbol of AND gate



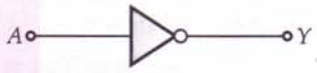
Truth table of AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

47. NOT gate. It is a digital circuit having only one input and one output. It gives a high output (1) if the input A is low (0) and vice versa. It is described by the Boolean expression,

$$\overline{A} = Y$$

Logic symbol of NOT gate



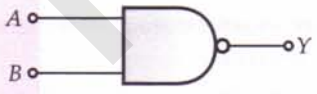
Truth table of NOT gate

A	B
0	1
1	0

48. NAND gate. It is obtained by connecting the output of an AND gate to the input of a NOT gate. Its input is high if both inputs A and B are not high. It is described by the Boolean expression,

$$\overline{A . B} = Y$$

Logic symbol of NAND gate



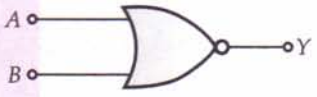
Truth table of NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

49. NOR gate. It is obtained by connecting the output of an OR gate to the input of a NOR gate. Its output is high if neither input A nor input B is high. It is described by the Boolean expression,

$$\overline{A + B} = Y$$

Logic symbol of NOR gate



Truth table of NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

50. XOR or exclusive OR gate. The XOR gate gives a high output if either input A or B is high but not when both A and B are high or low. It can be obtained by using a combination of two NOT gates, two AND gates and one OR gate. It is described by Boolean expression : $Y = \overline{A}B + A\overline{B}$

The XOR gate is also known as *difference gate* because its output is high when the inputs are different.

Logic symbol of XOR gate

Truth table of XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

51. Integrated circuits (ICs). A miniature electronic circuit, consisting of many passive components like R and C and active components like diode and transistor, fabricated within a single semiconductor chip is called an integrated circuit. ICs are obtained by a complex procedure involving diffusion, oxidation, photolithography, metallisation, etc. These circuits have revolutionised the electronic industry.